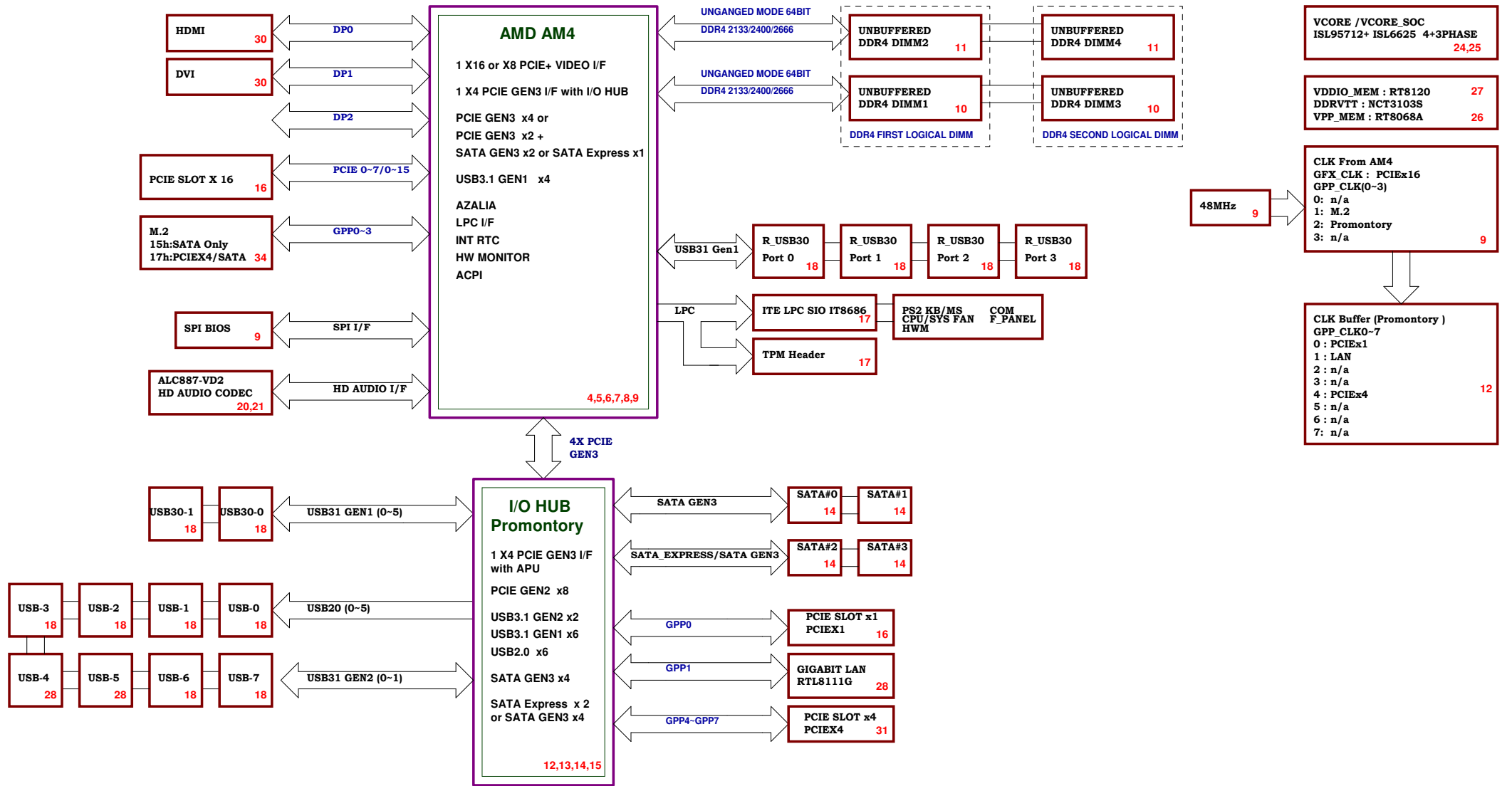
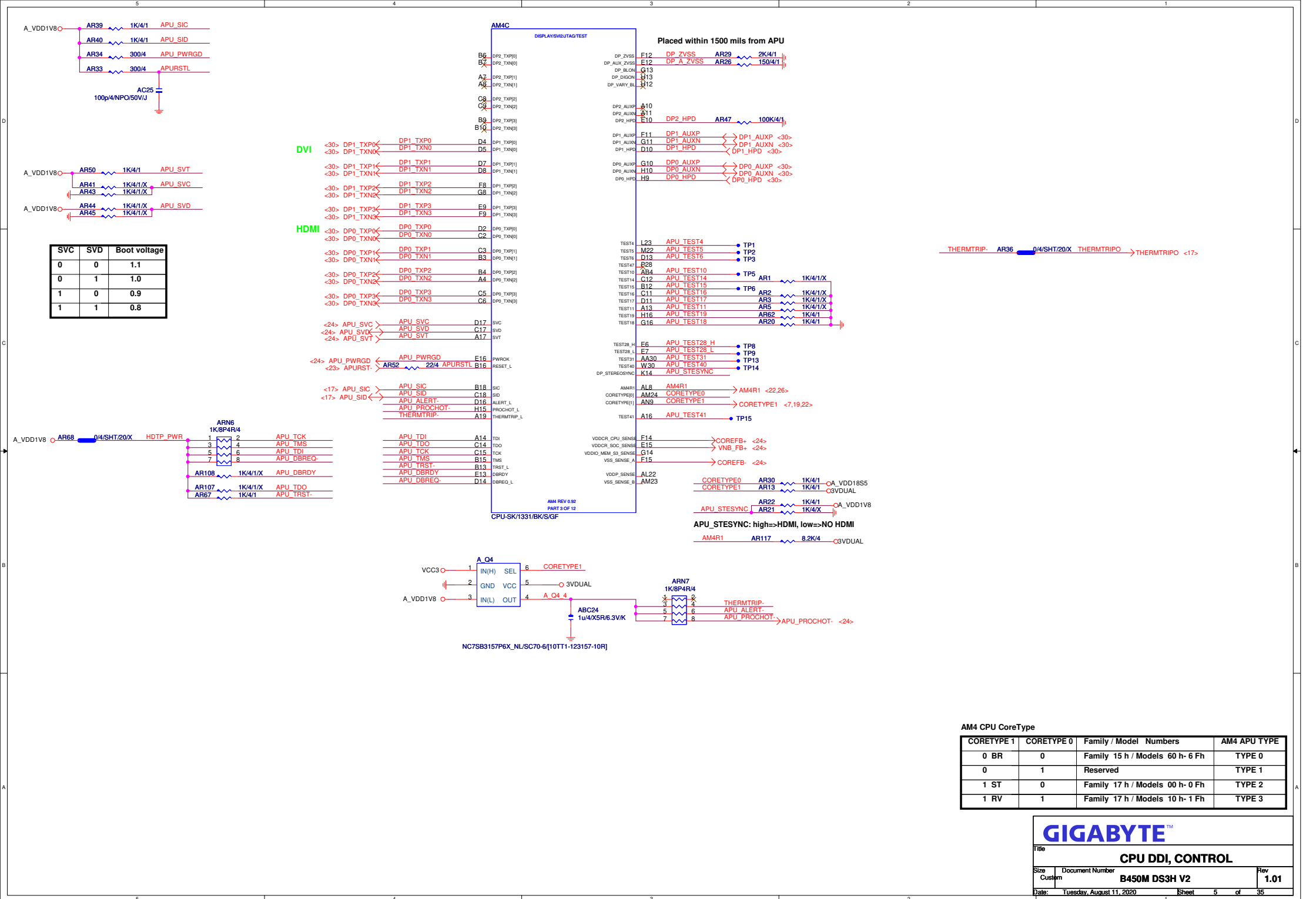
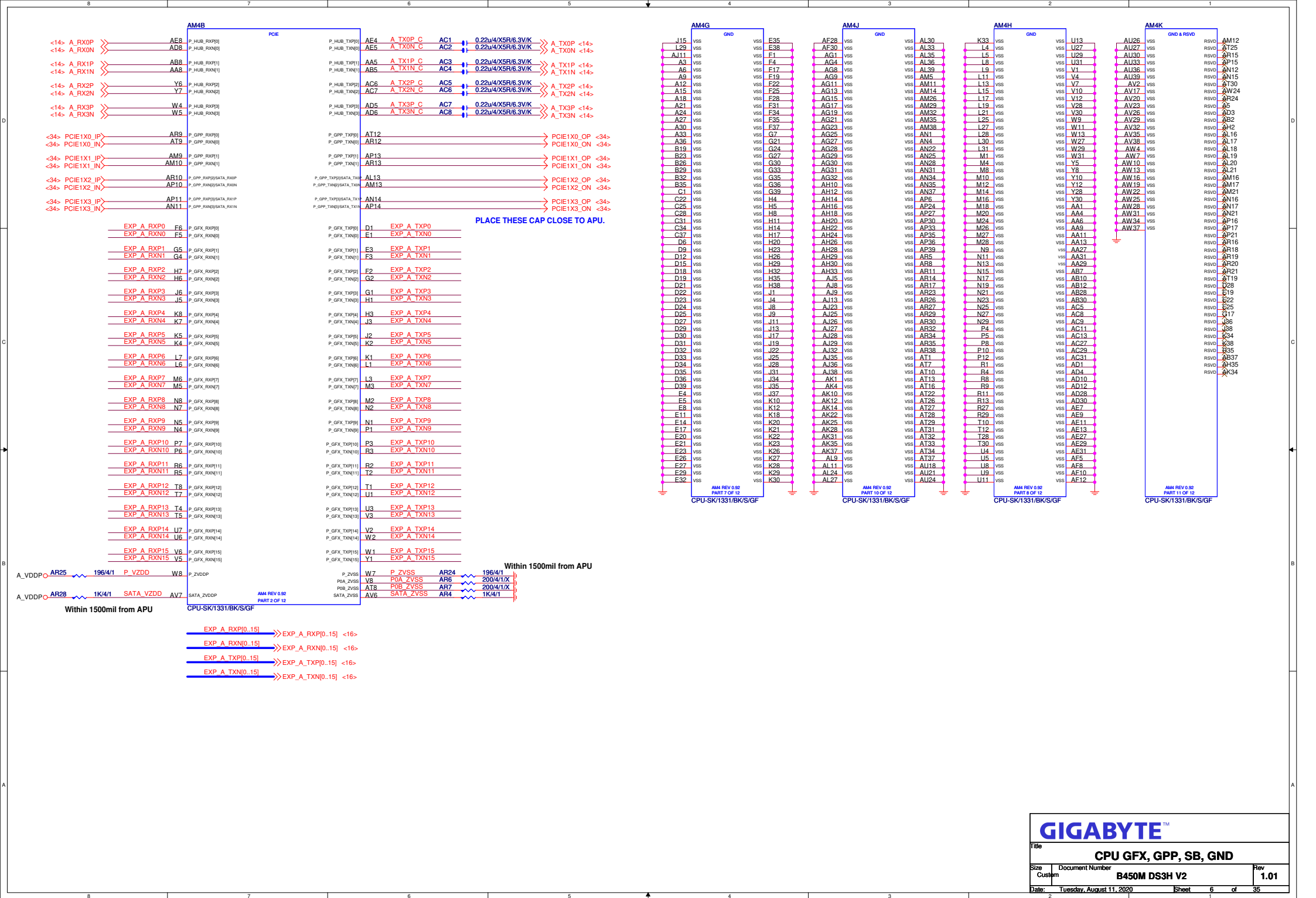


5					4					3					2					1																			
B450M DS3H V2																																							
PAGE					TITLE					Revision :1.01																													
01	COVER SHEET				26	PM PWR,VPP_MEM,VDDCR_SOC_S5																																	
02	BOM & PCB MODIFY HISTORY				27	DDR POWER ,5VDUAL ,3VDUAL																																	
03	BLOCK DIAGRAM				28	RTL8111G																																	
04	CPU DDR4 MEMORY				29	FAN, COM, HWM																																	
05	CPU DDI, CONTROL				30	HDMI, DVI Connector																																	
06	CPU GFX, GPP, SB, GND				31	PCIEx4 Slot																																	
07	CPU MISC				32	CPU SMD CAP BOTTOM																																	
08	CPU POWER				33	CPU SMD CAP TOP																																	
09	CPU CLK, USB3, SPI ,LPC				34	M.2 Socket (SATA/PCIE)																																	
10	DDR4 CHANNEL A				35	Audio LED																																	
11	DDR4 CHANNEL B																																						
12	PM CLK, SPI, MISC																																						
13	PM USB																																						
14	PM SATA, GPP																																						
15	PM POWER, GND																																						

<





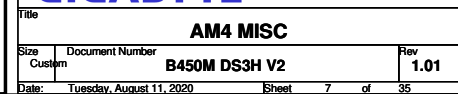
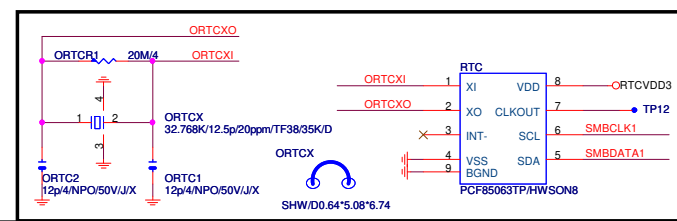


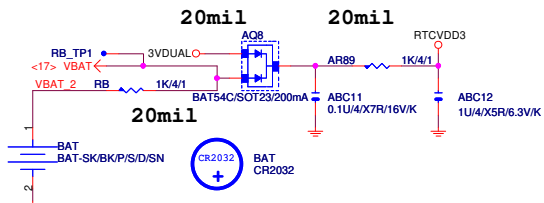
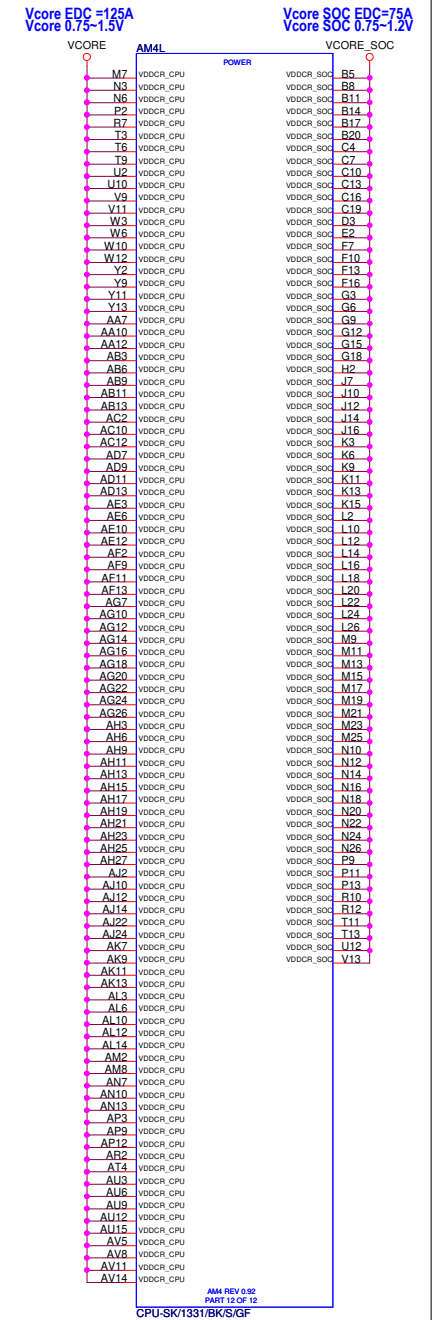
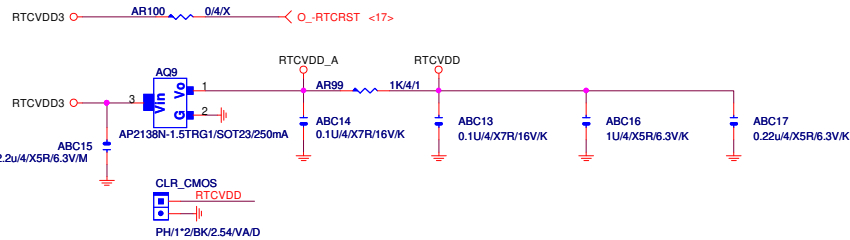
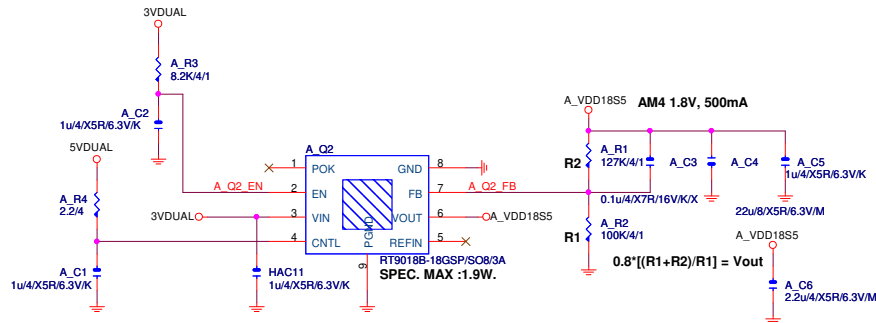
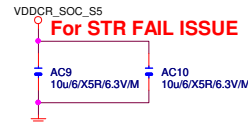
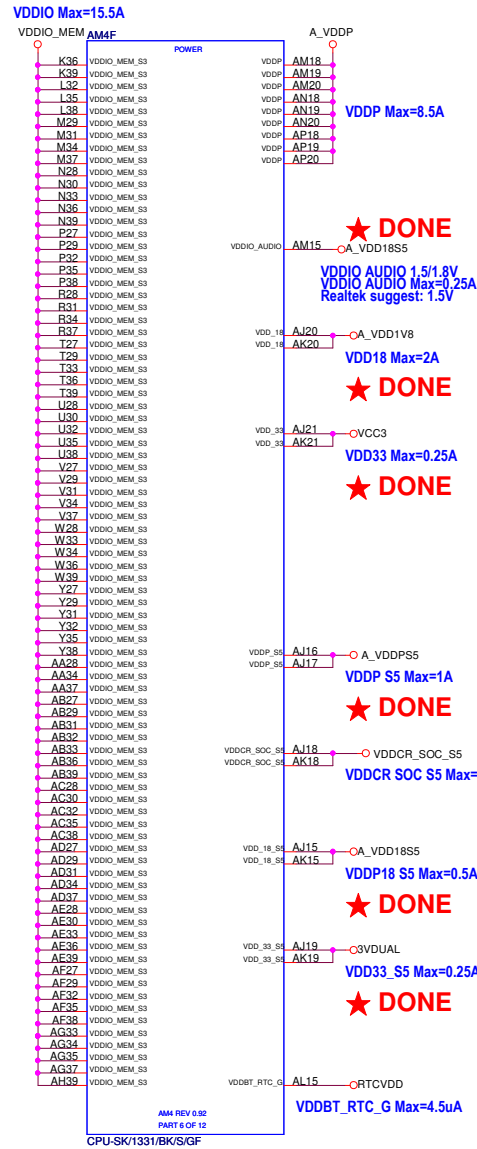
GIGABYTE™

Title				CPU GFX, GPP, SB, GND			
Size				Document Number			
Customer				B450M DS3H V2			
Date:				Tuesday, August 11, 2020			
Sheet				6 of 35			
Rev				1.01			

Internal Debug Only

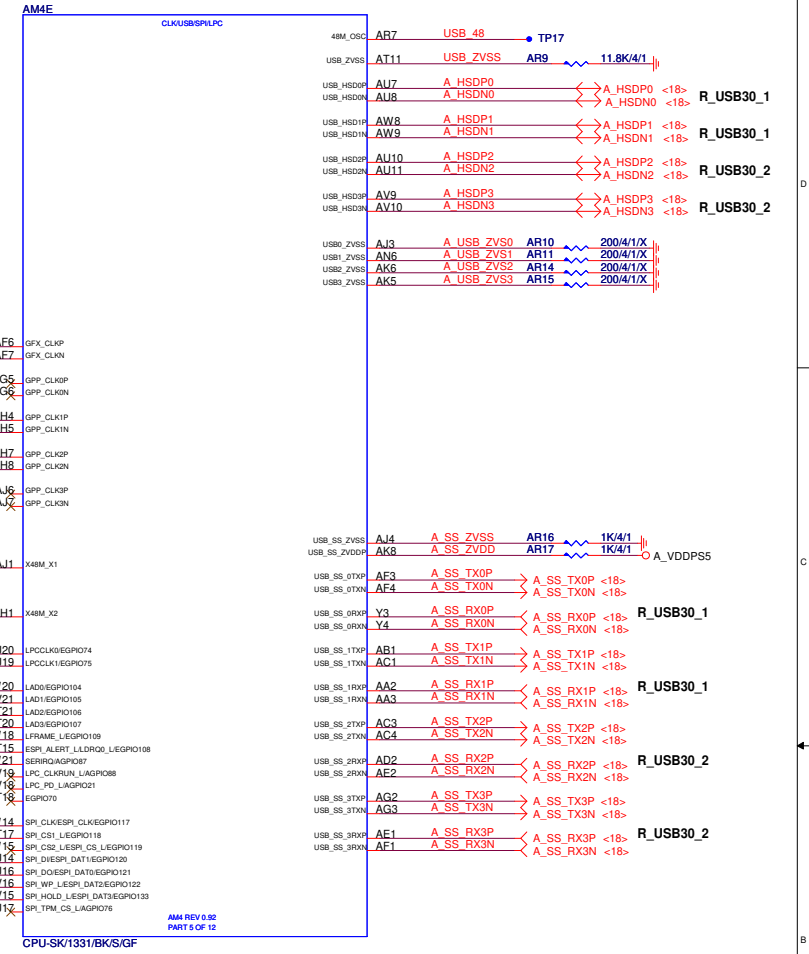
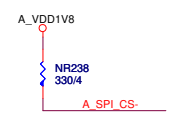
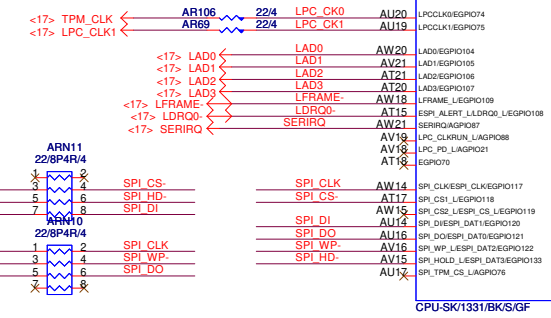
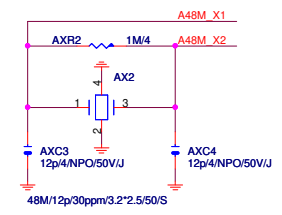
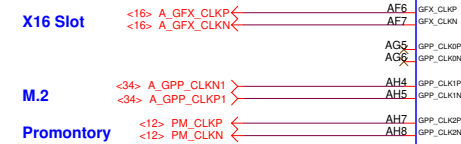
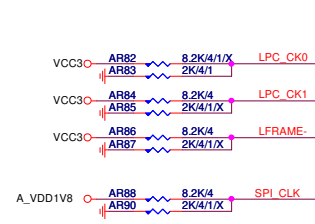
TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.





CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	

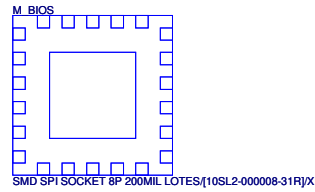
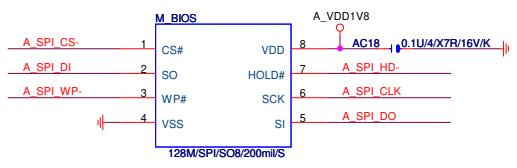
GIGABYTE™		
Title CPU POWER		
Size Custom	Document Number B450M DS3H V2	Rev 1.01
Date: Tuesday, August 11, 2020	Sheet 8	of 35



128Mb: 128M/SPI/SO8/200mil/S

256Mb: 256M/WSON8/200MIL/S

Footprint: IC8WSON-BIOS-COLAY

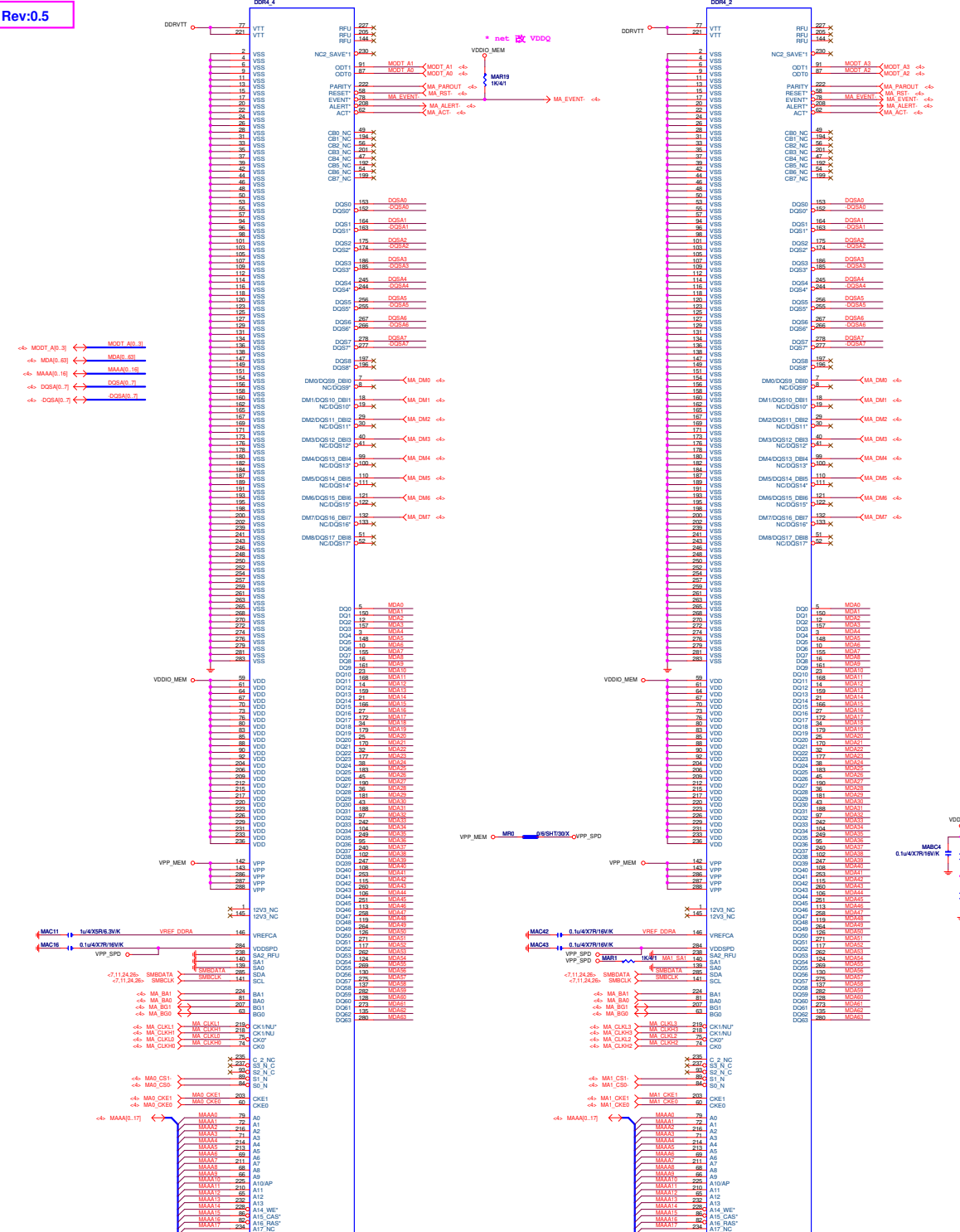


GIGABYTE™

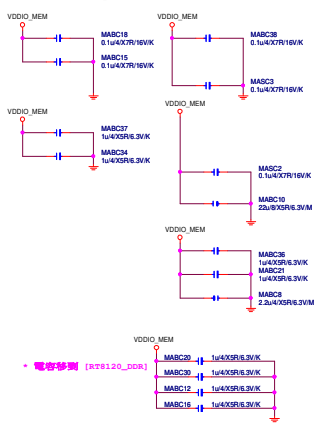
TitleCPU USB3, SPI

SizeCustomDocument NumberB450M DS3H V2Rev1.01

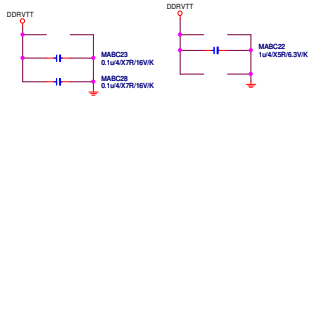
DateTuesday, August 11, 2020Sheet9 of 35



DDR12V Decouple



DDRVT Decouple



CHANNEL A0
SA2:0=000

CHANNEL A1
SA2:2=010

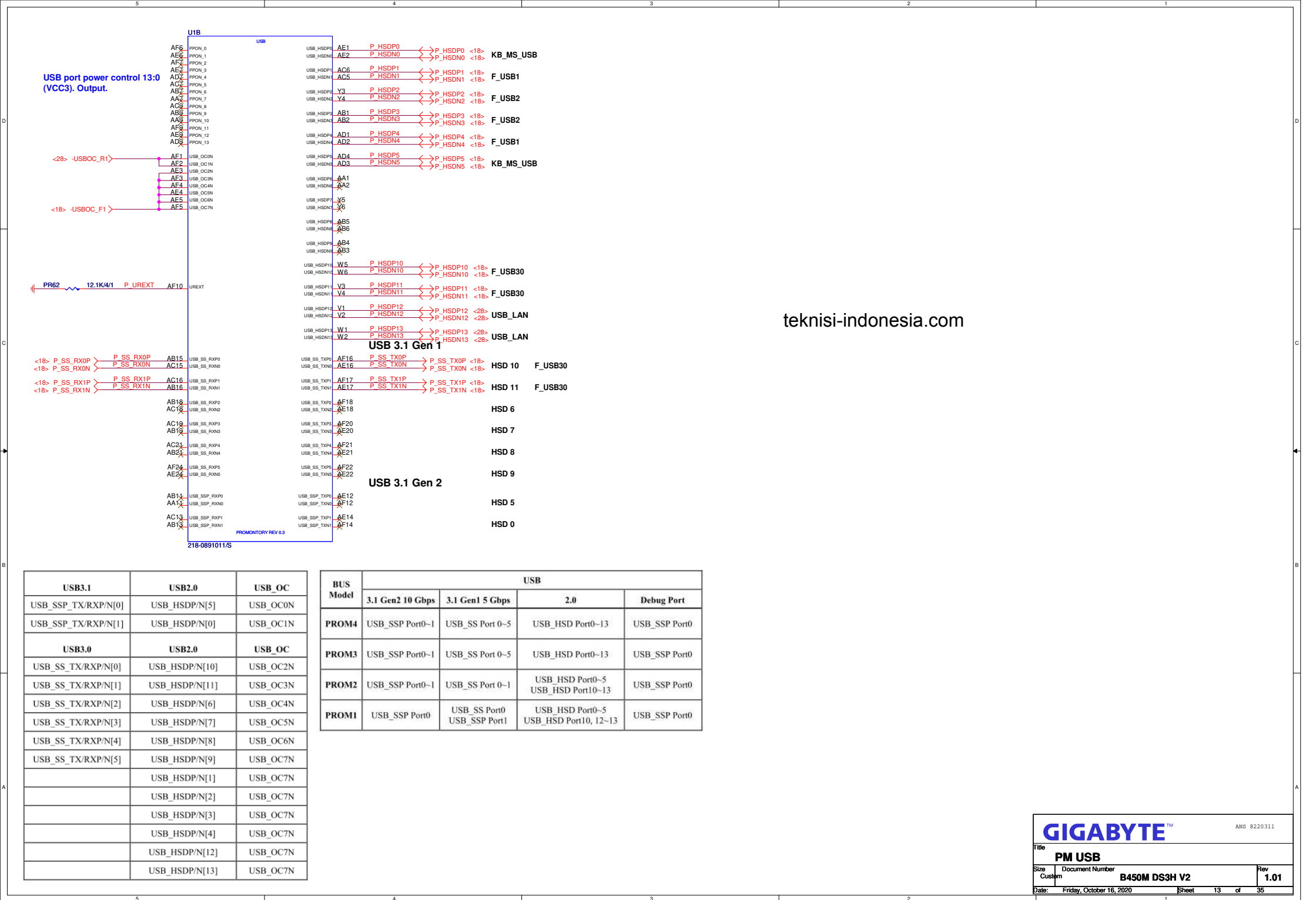


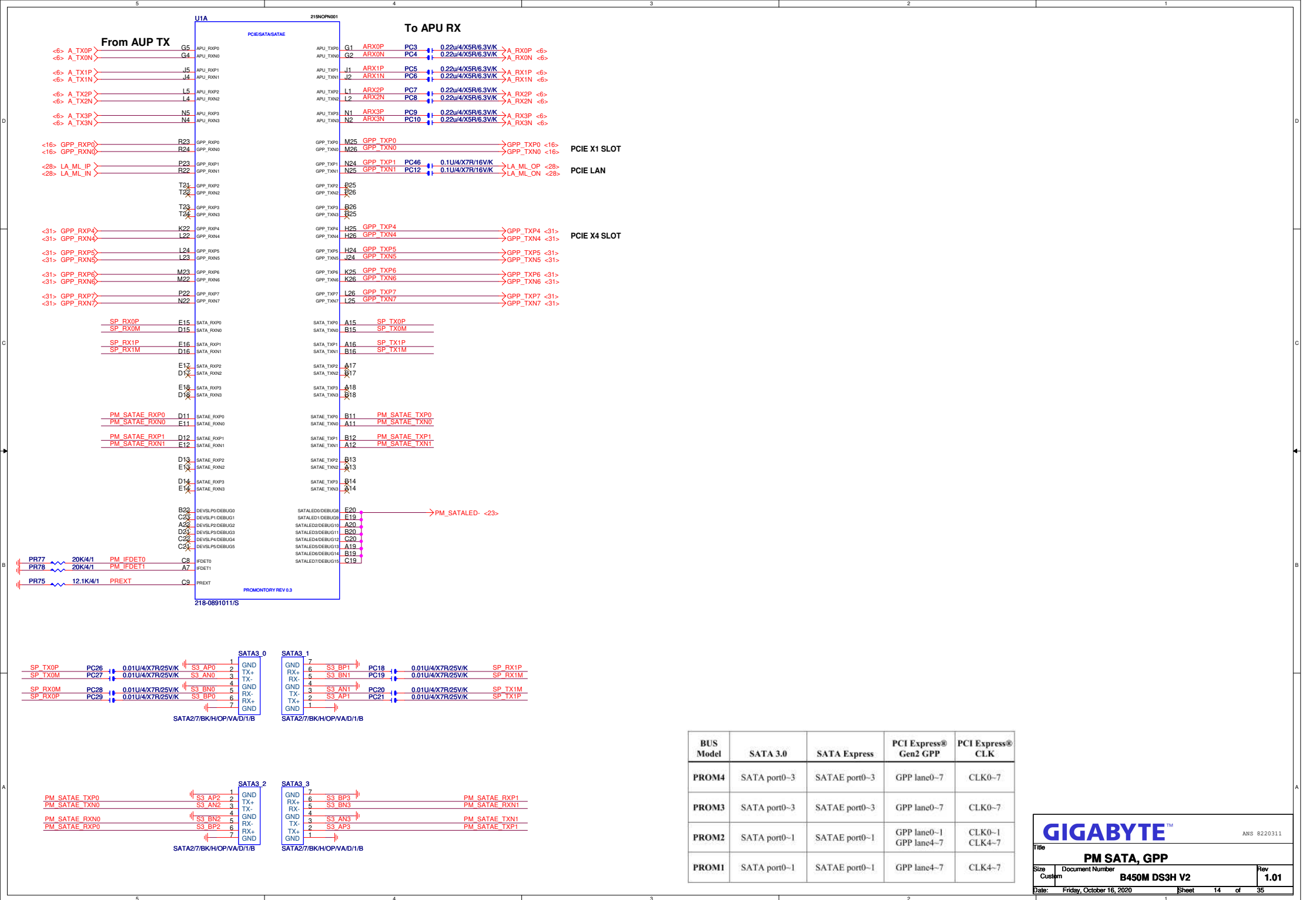
CHANNEL B0
SA2:1=001

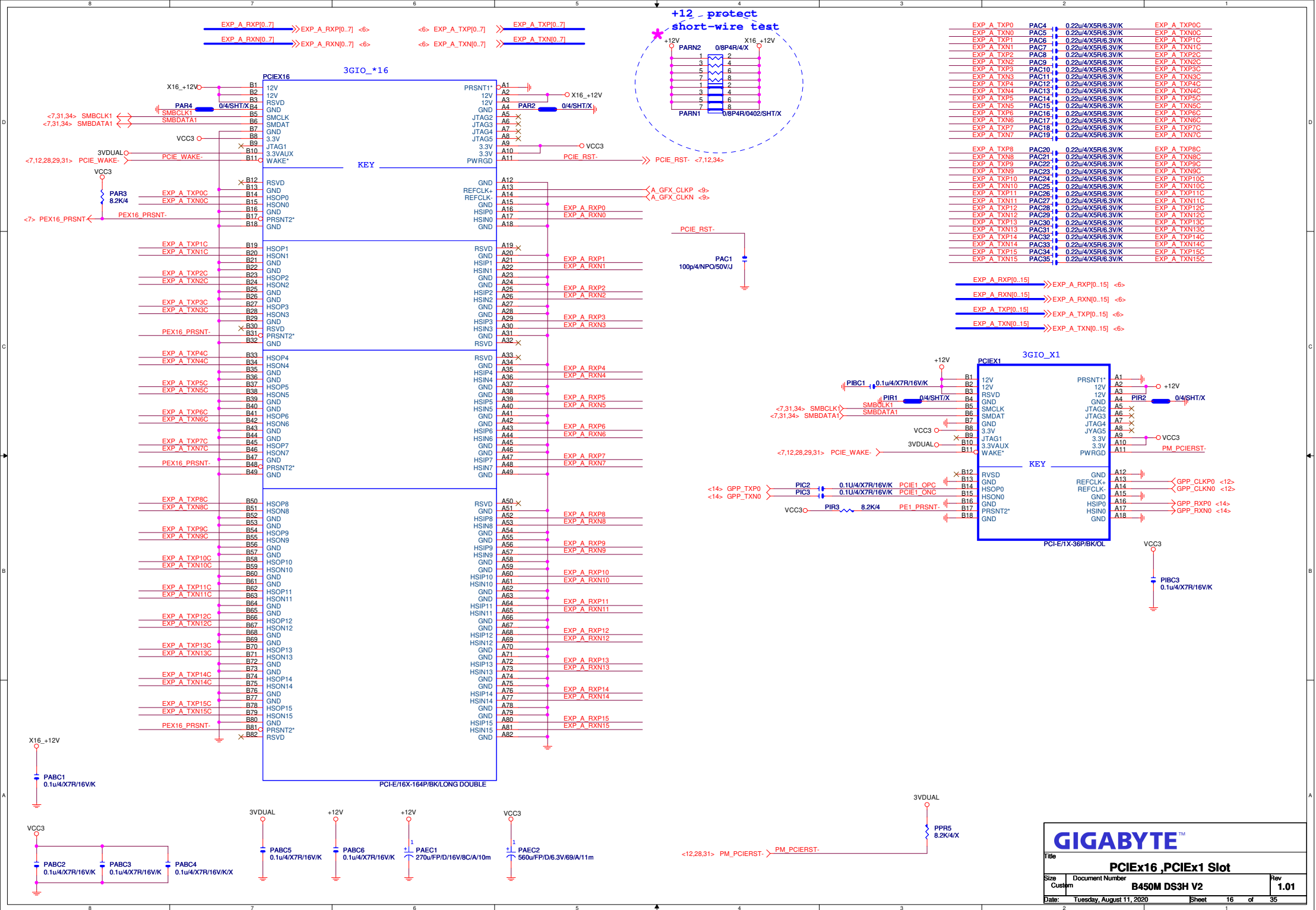


CHANNEL B1
SA2:3=011

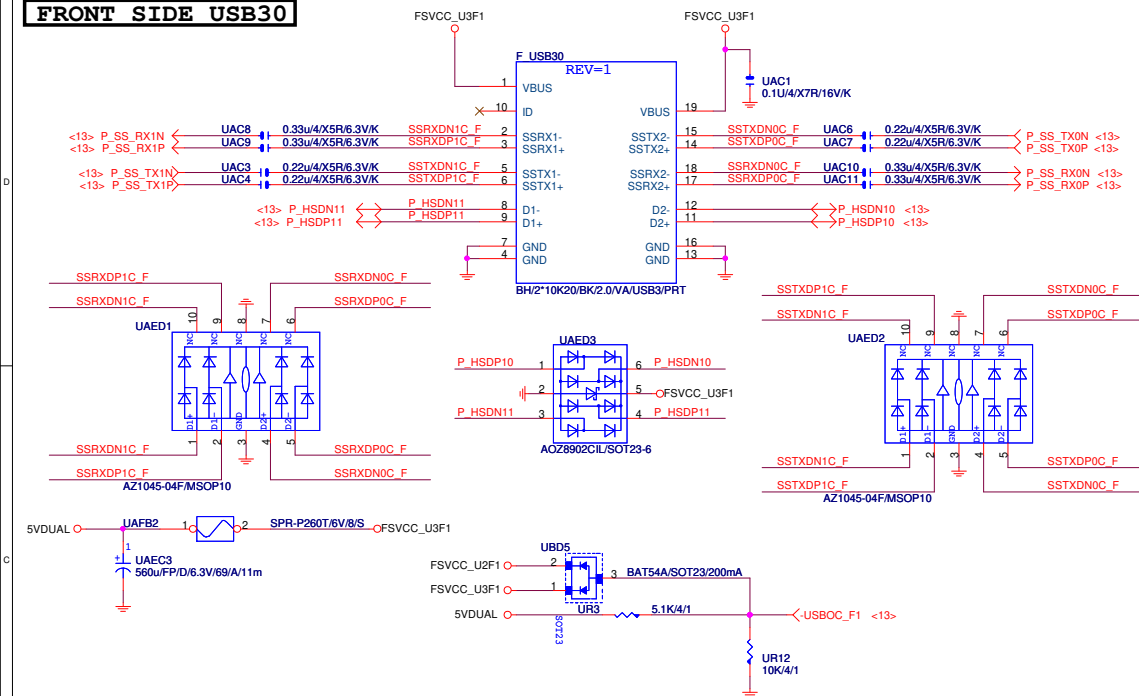
GIGABYTE		
DDR4 CHANNEL B		
File	Document Number	Rev
Size	B450M D3SH V2	1.01
Created	Monday, August 11, 2020	Page 11 of 35



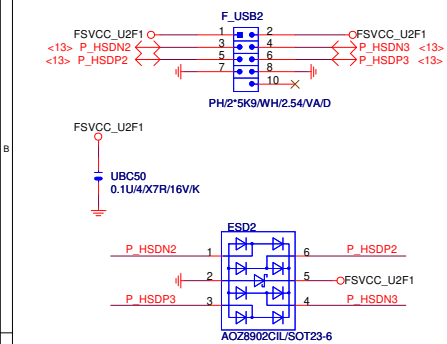




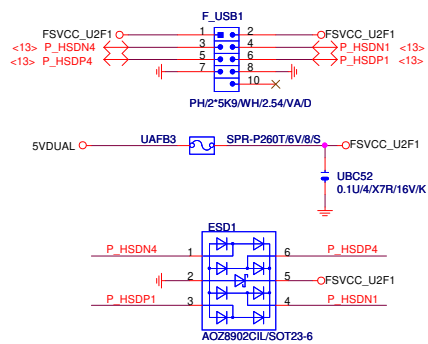
FRONT SIDE USB30



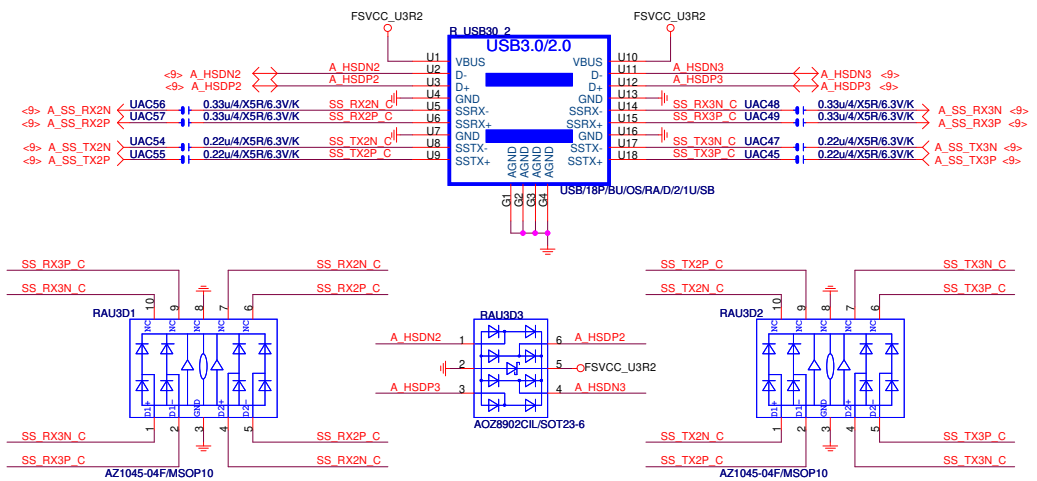
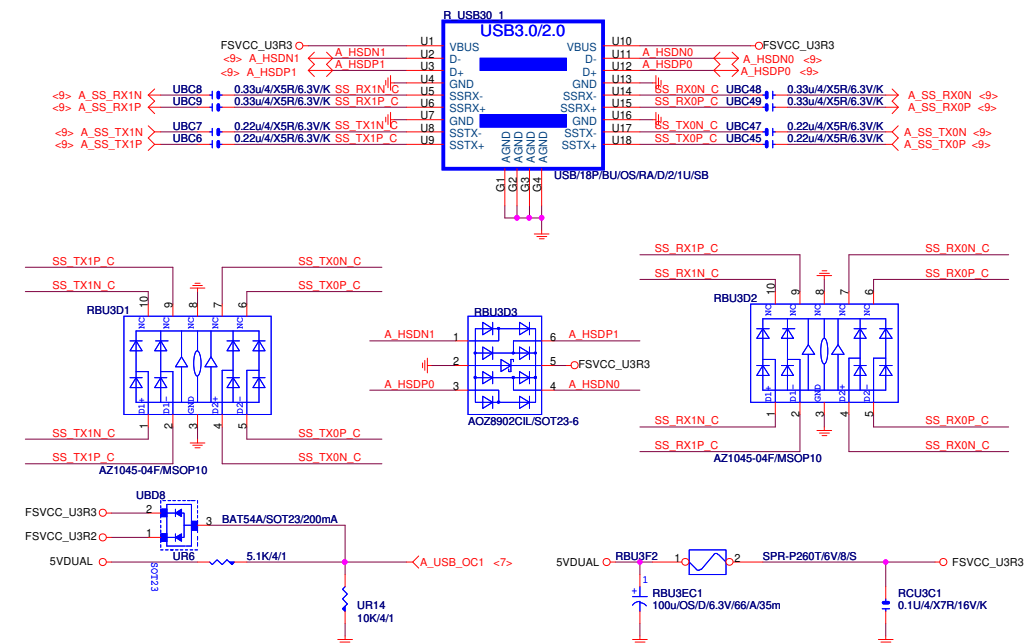
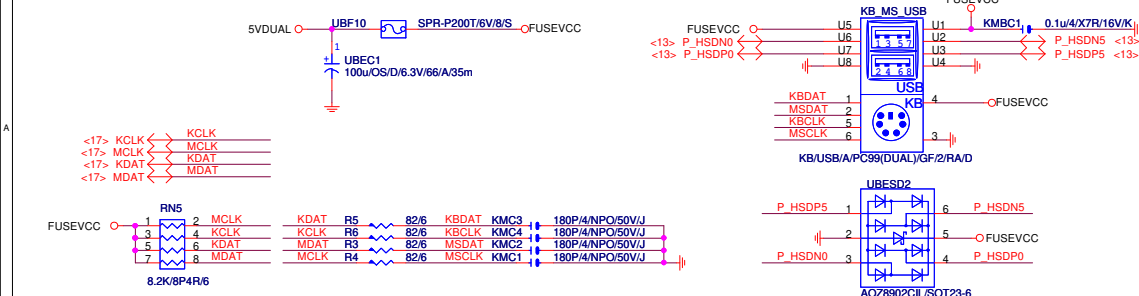
FRONT SIDE USB2



FRONT SIDE USB1

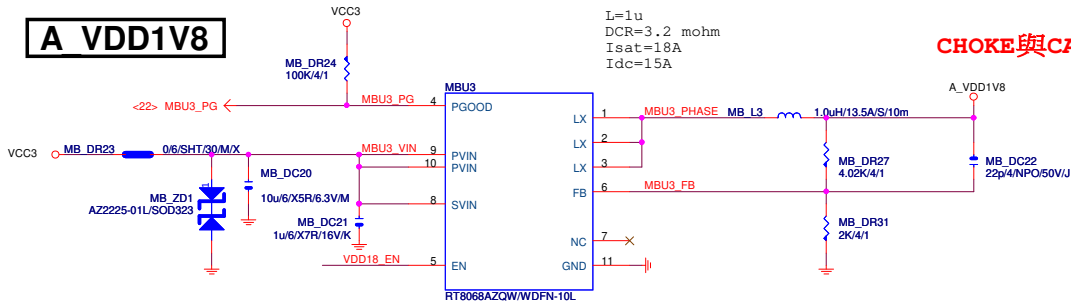


KB/MS & USB



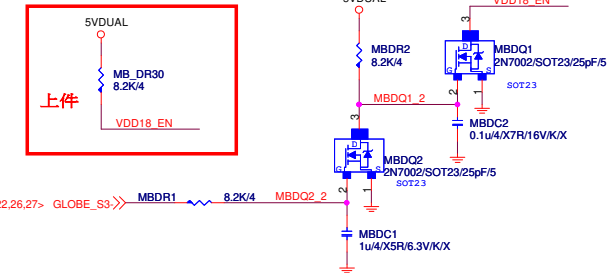
REV: 0.4

A VDD1V8



PWR_SEQ

* 刪 MA_DR32

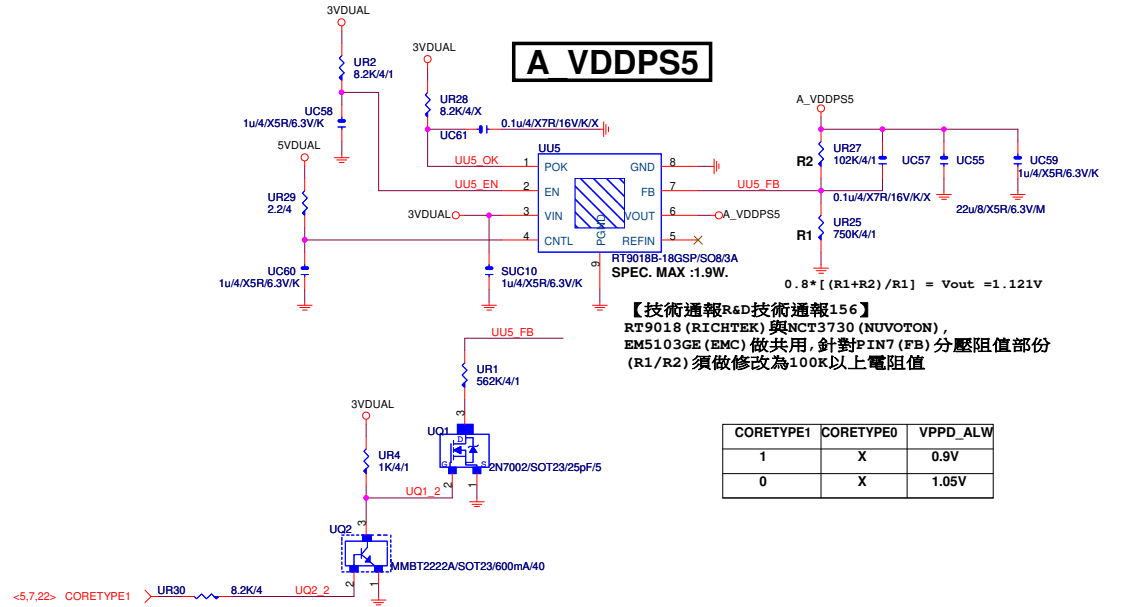


VPP CAP

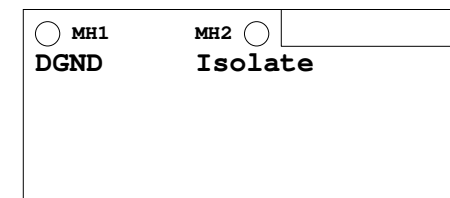
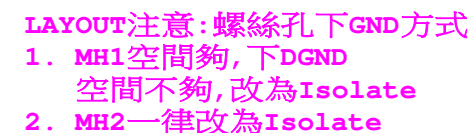
* 大電容 x0

47u*1PCS

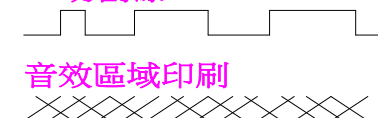
A VDDPS5



CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

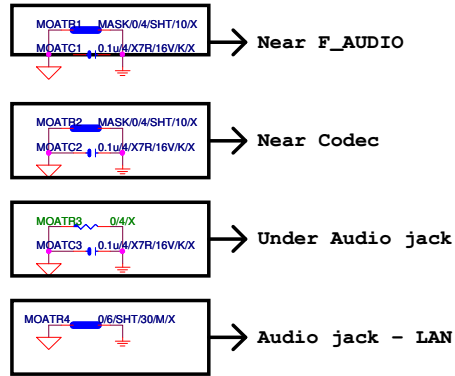


GND切割線

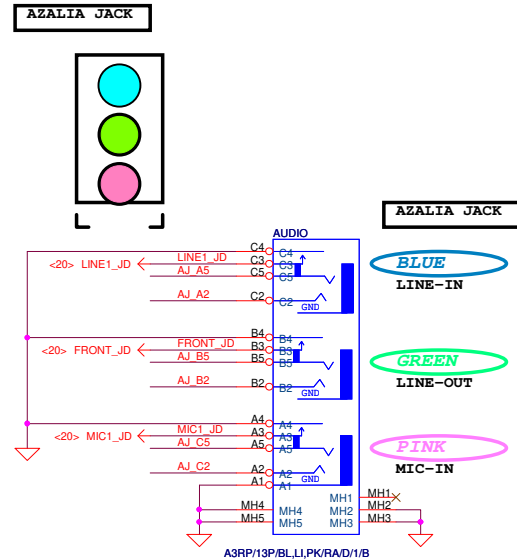
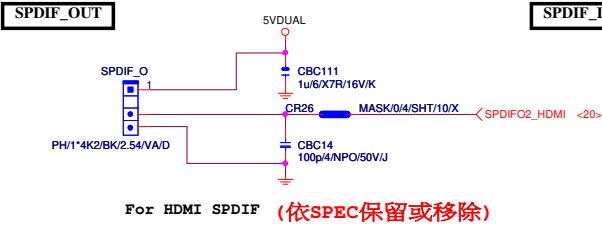


GIGABYTE™			
Title ALC887 CODEC			
Size Custom	Document Number B450M DS3H V2		Rev 1.01
Date:	Tuesday, August 11, 2020	Sheet	20 of 35

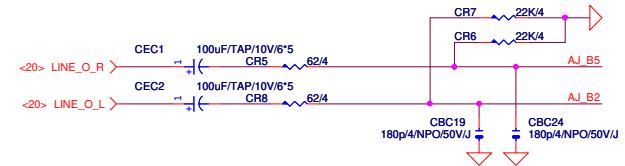
Rev 3.1



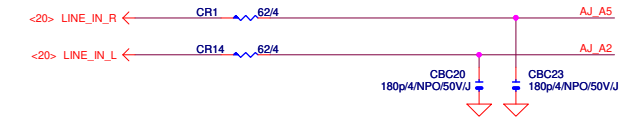
*量産前, 0ohm改short pad



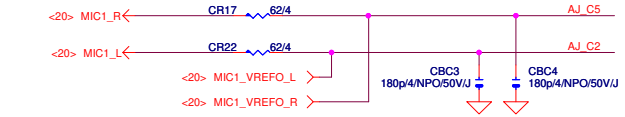
LINE-OUT



LINE-IN



MIC-IN

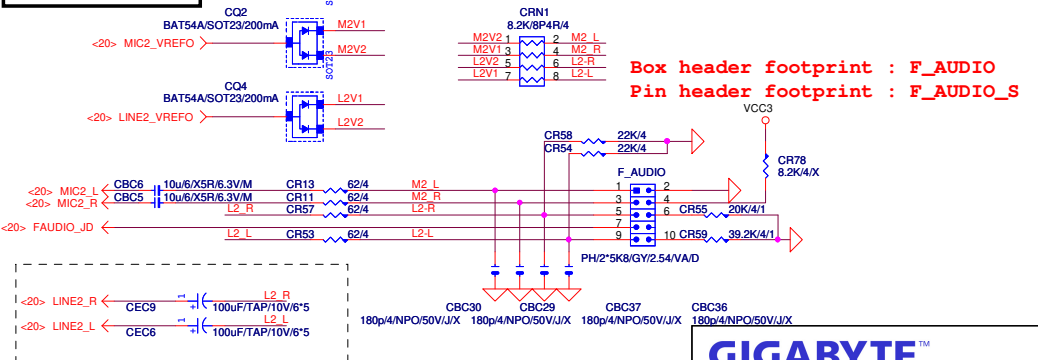


SURROUND

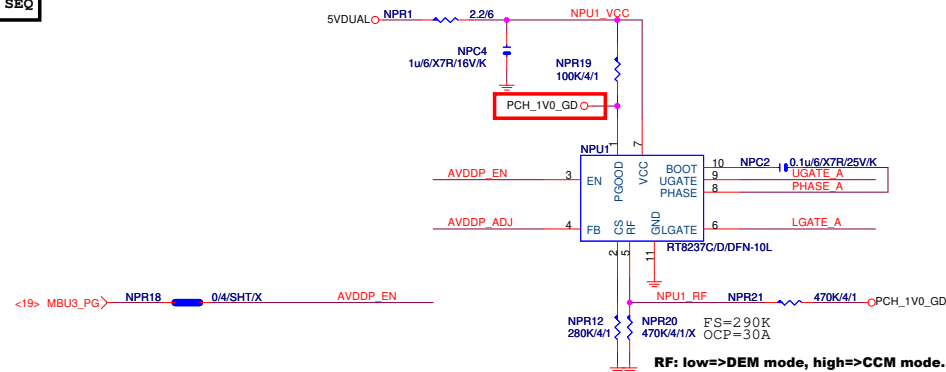
CEN/LFE

SURR BACK

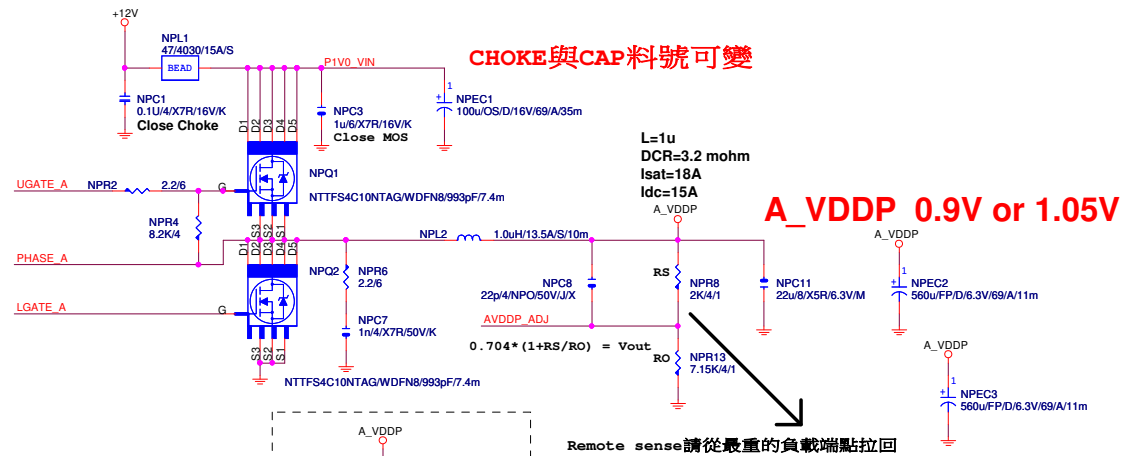
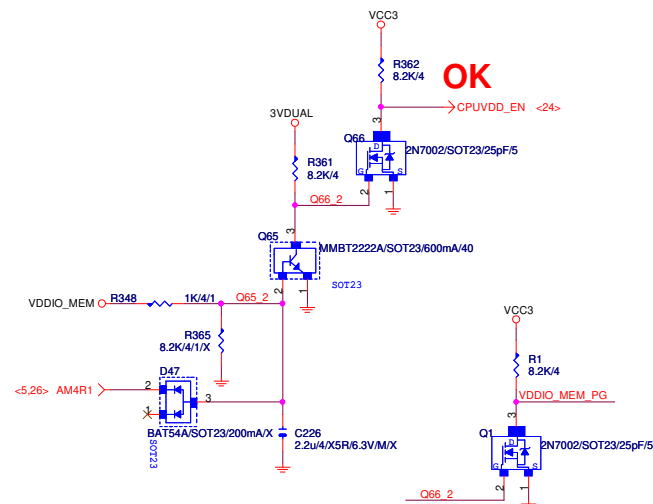
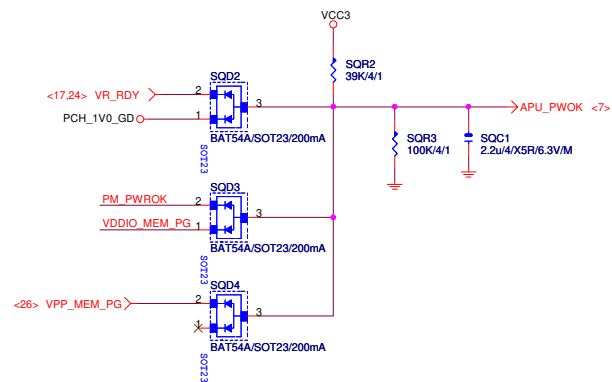
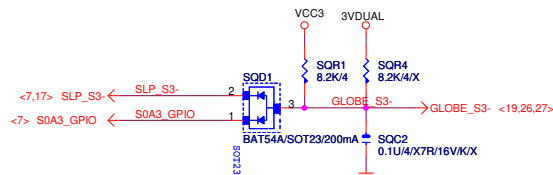
AZALIA FRONT PANEL



GIGABYTE™			
Title			
AUDIO JACK			
Size	Document Number	Rev	
Custom	B450M DS3H V2	1.01	
Date:	Tuesday, August 11, 2020	Sheet	21 of 35



<19> MBUS3_PG> NPR18 0/4/SHT/X AVDDP_EN

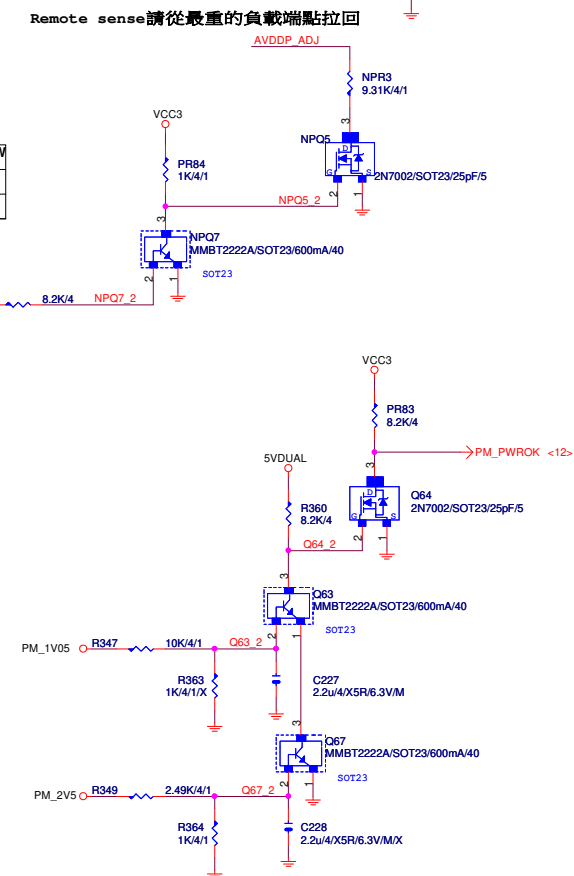


CHOKE與CAP料號可變

A_VDDP 0.9V or 1.05V

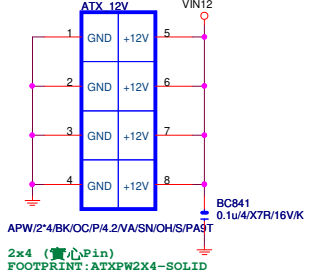
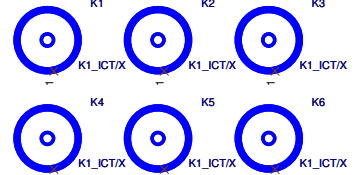
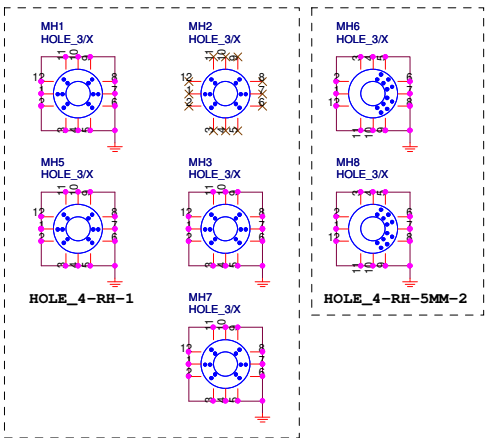
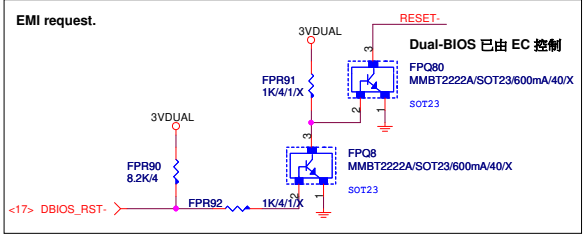
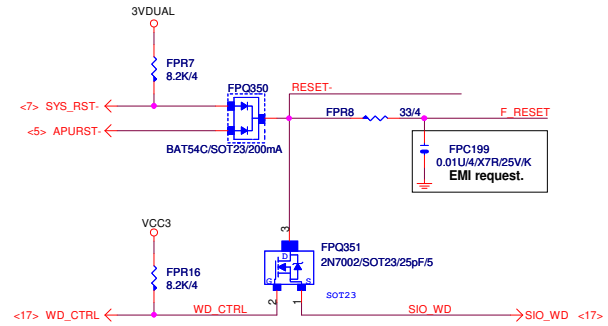
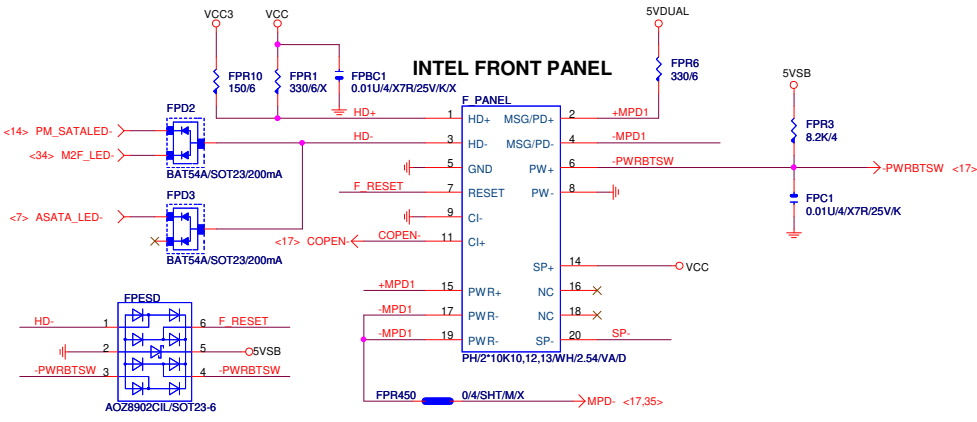
CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

<5,7,19> CORETYPE1 CORETYPE1 PR85 8.2K/4 NPO7 2

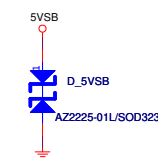
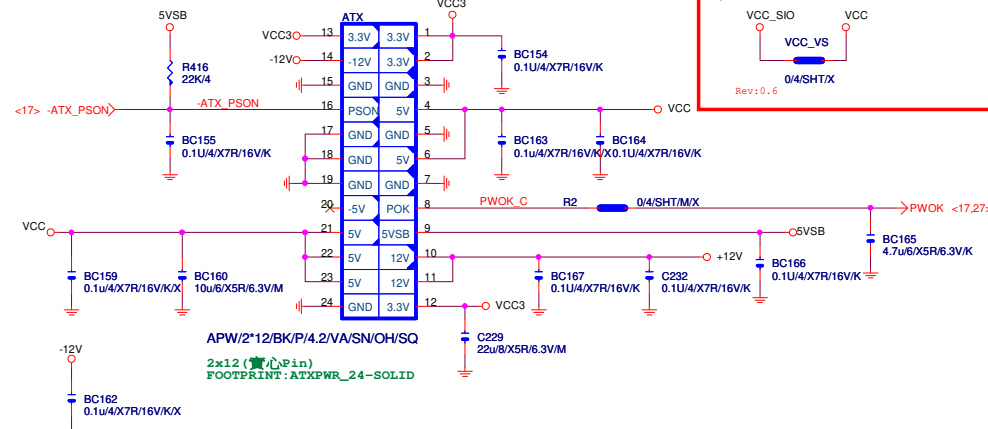
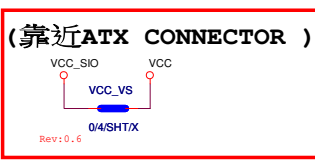


GIGABYTE™

POWER SEQ, A_VDDP		
Title	Document Number	Rev
Size	B450M DS3H V2	1.01
Date:	Tuesday, August 11, 2020	Sheet 22 of 35

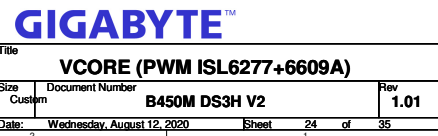


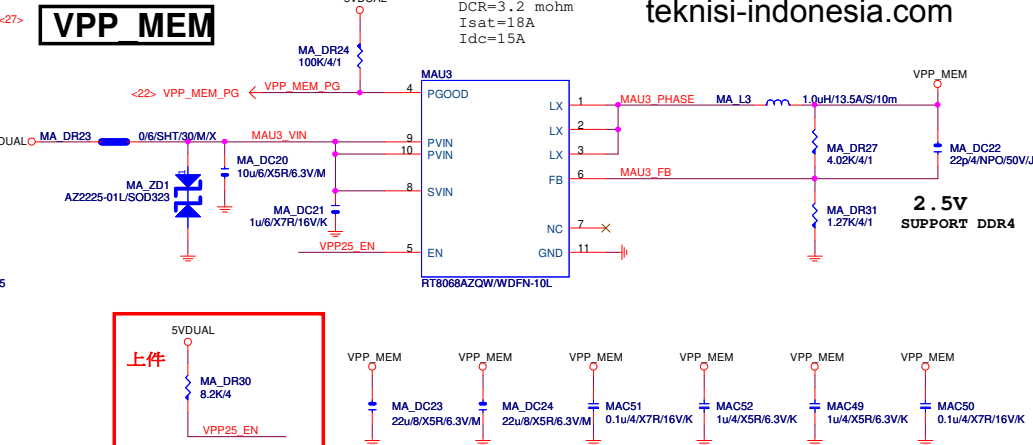
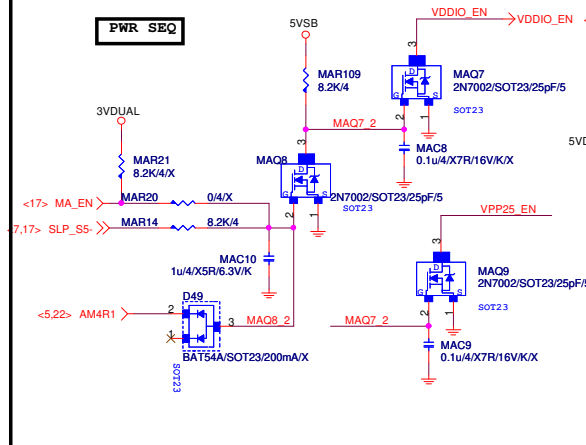
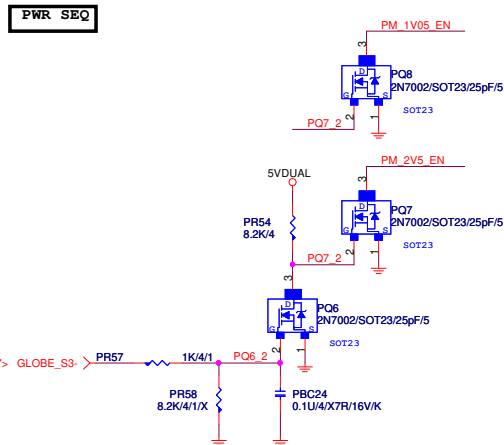
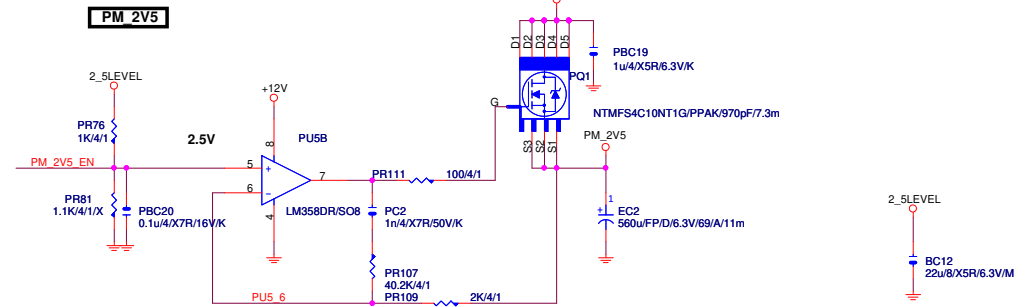
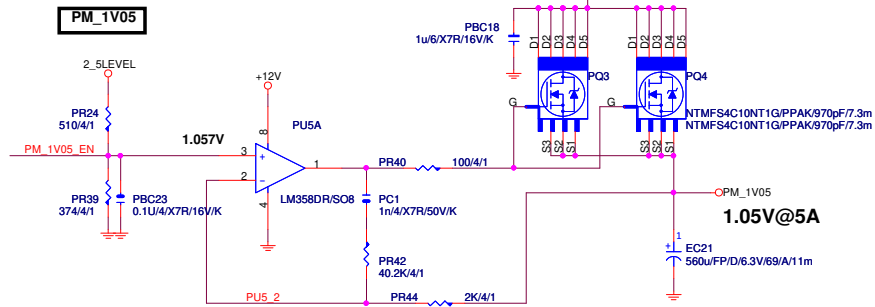
ATX POWER CONNECTOR



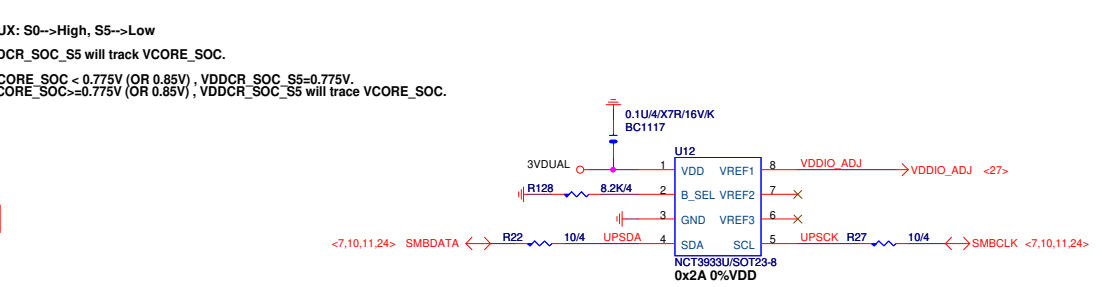
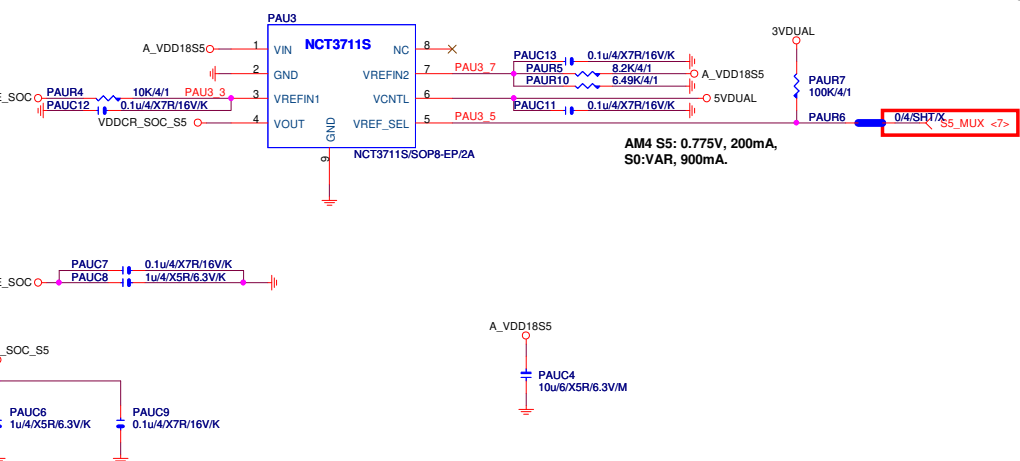
ATX_F_PANEL

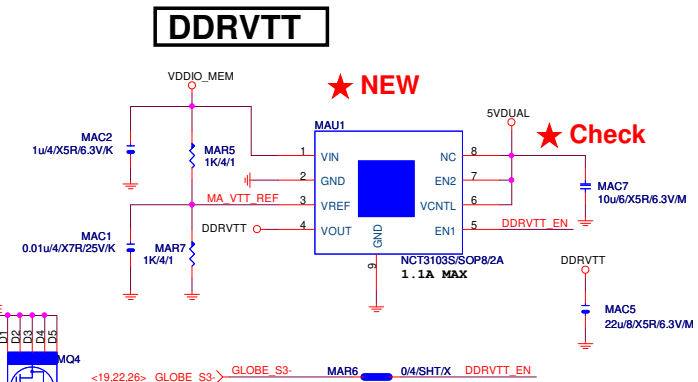
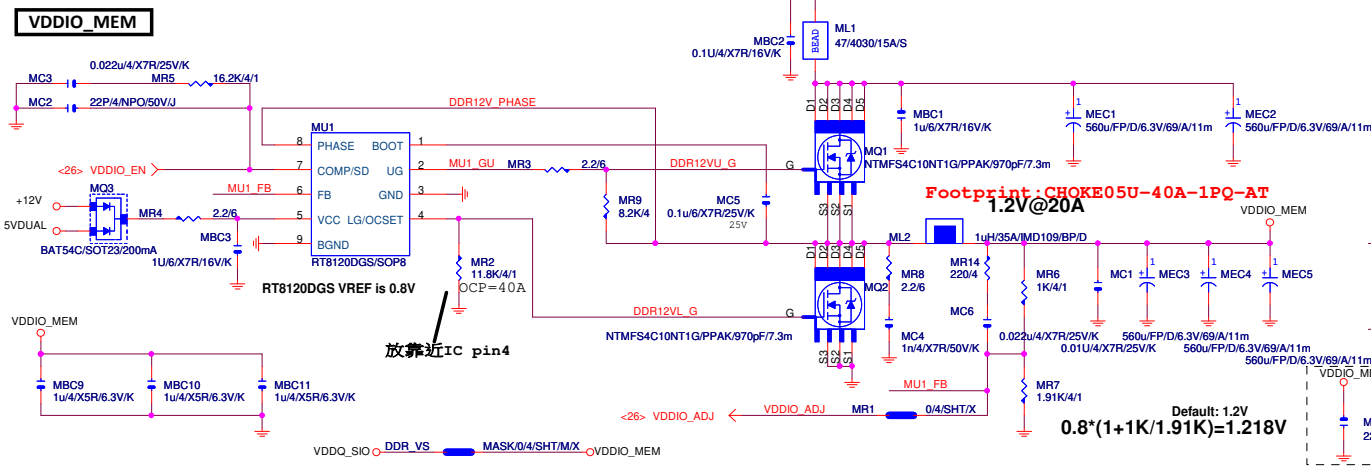
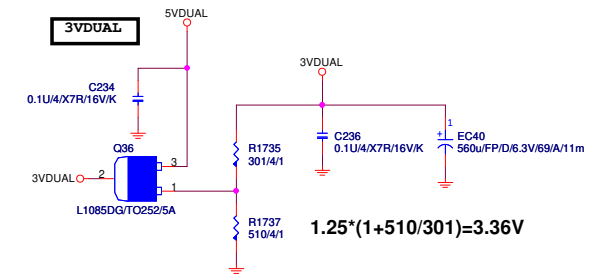
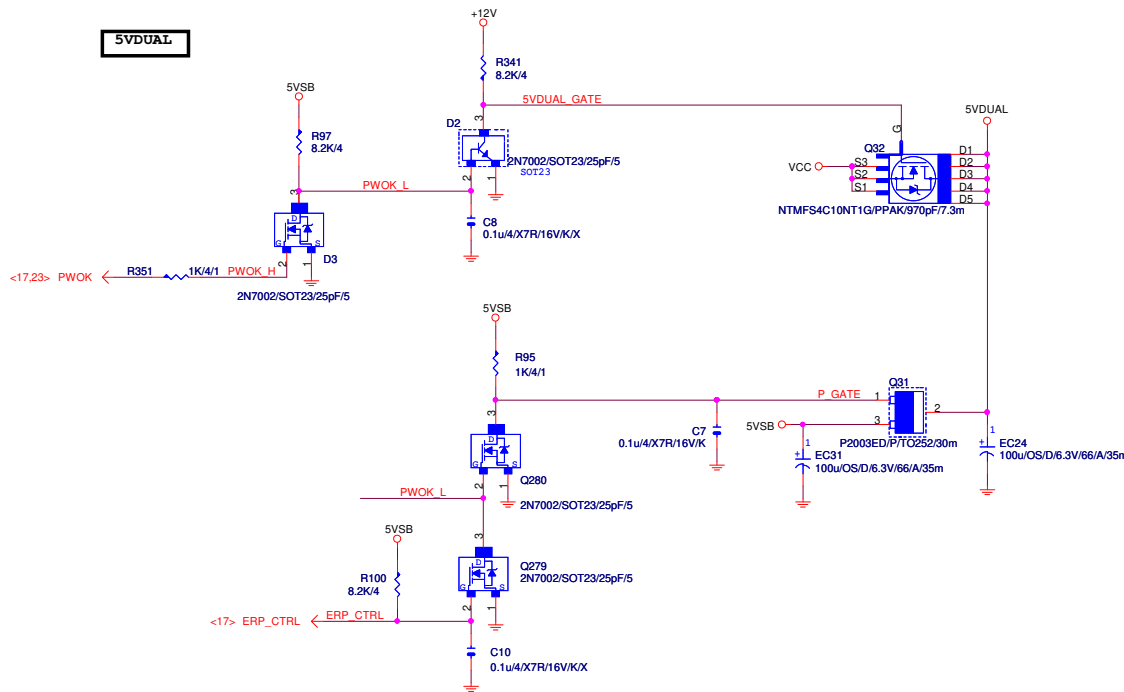
Size Custom
Document Number B450M DS3H V2
Date Tuesday, August 11, 2020
Rev 1.01
Sheet 23 of 35





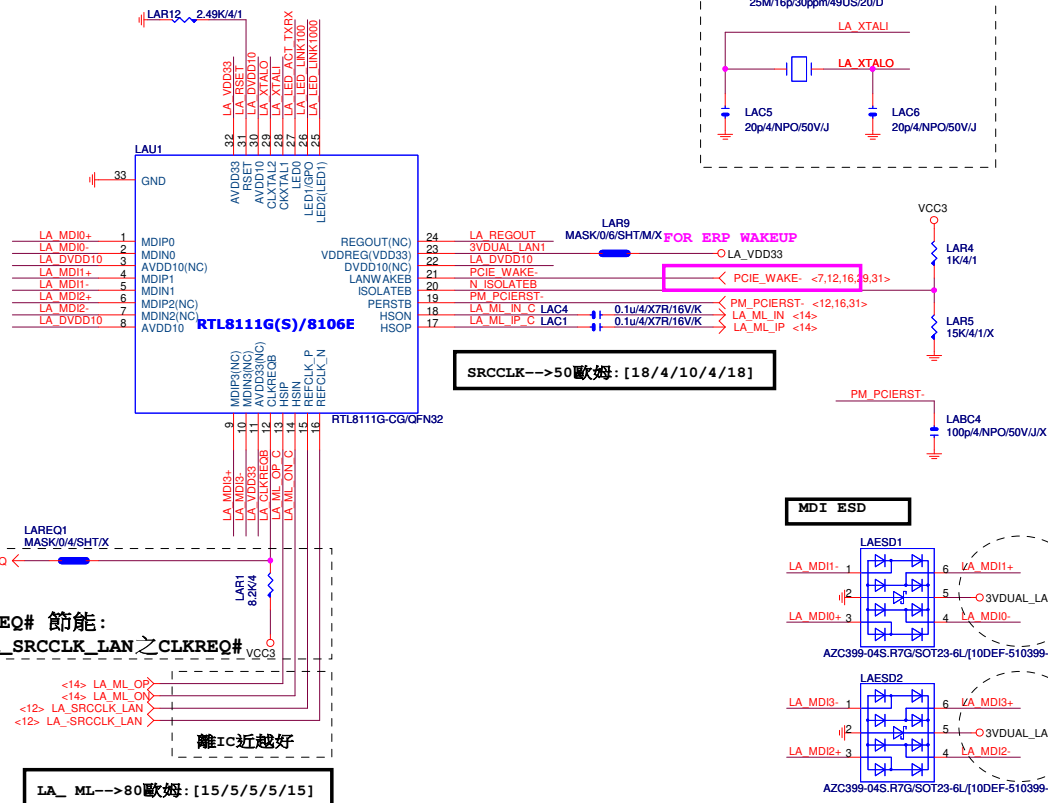
VDDCR SOC S5





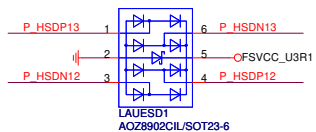
GIGABYTE™			
Title			
DDR POWER_5VDUAL			
Size	Document Number	Rev	
Custom	B450M DS3H V2	1.01	
Date:	Tuesday, August 11, 2020	Sheet	27 of 35

LAN:RTL8111G	R2.03
--------------	-------

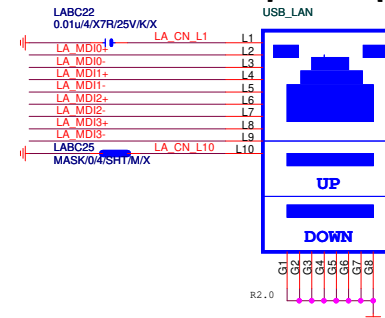


USB_LAN CONNECTOR	R2.03
-------------------	-------

RMA ESD PROTECT

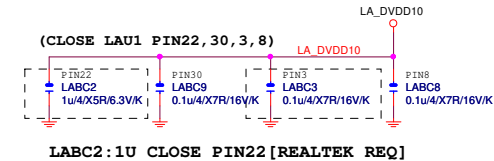


USB_LAN CONNECTOR



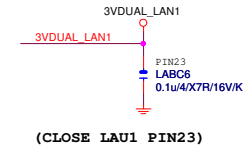
LA_MDI-->100歐姆:[20/4/8/4/20]

LAN POWER

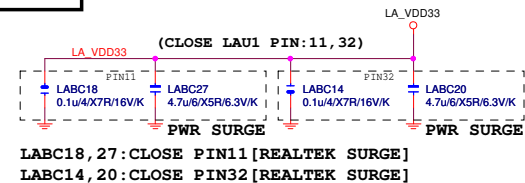


LAN POWER

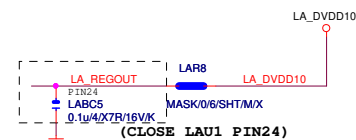
note: lan power連接及電流



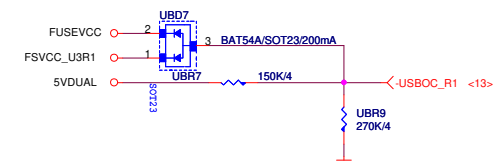
LAN POWER



LAN POWER



teknisi-indonesia.com



USB POWER



Close to connector
USB_LAN 2-Port 2.0A
FUSE-0805

LAN POWER

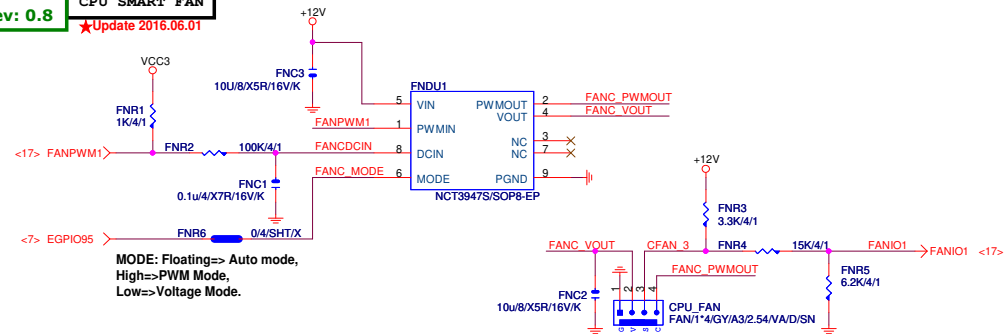


EMI

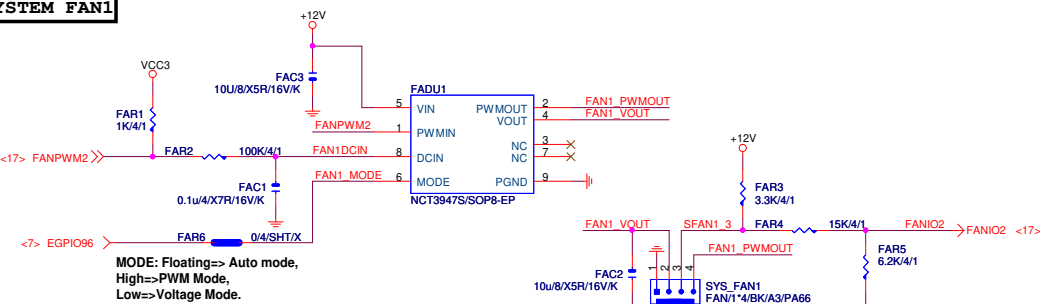
LAN AGND change GND
Remove Short Pad

GIGABYTE™

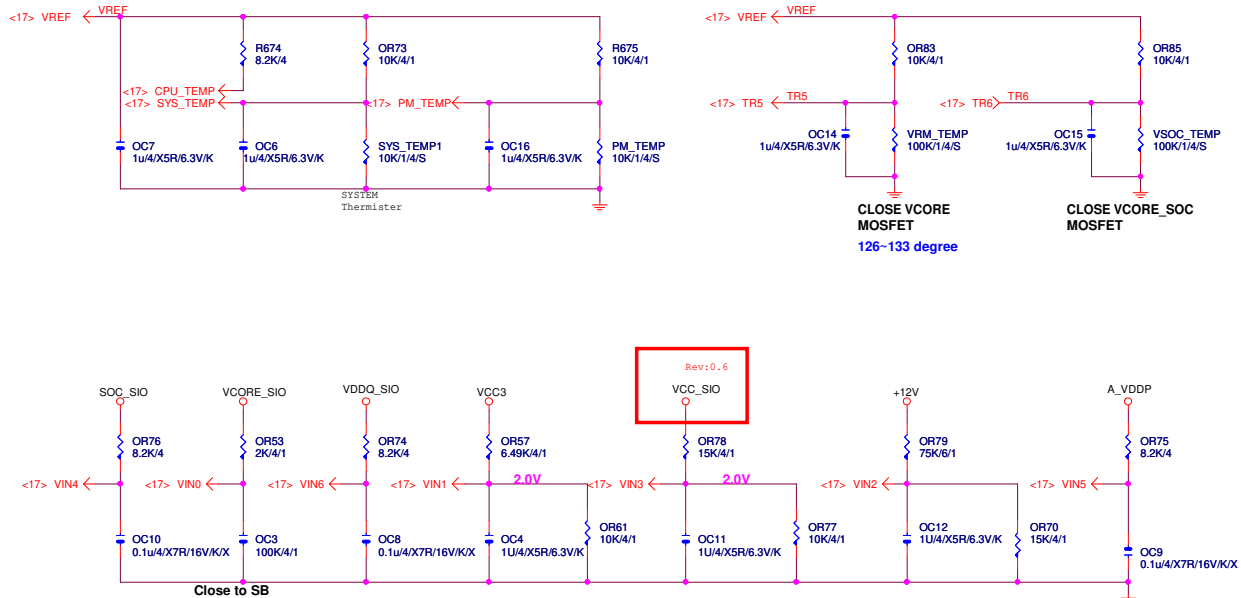
Title			
RTL8111G			
Size	Document Number	Rev	
Custom	B450M DS3H V2	1.01	
Date:	Tuesday, August 11, 2020	Sheet	28 of 35



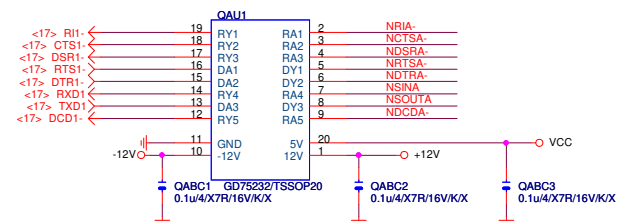
SYSTEM FAN1



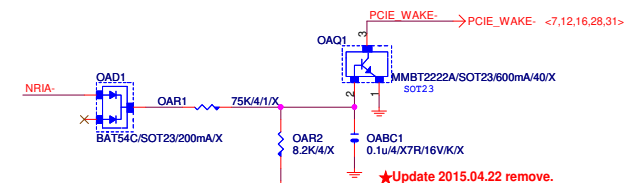
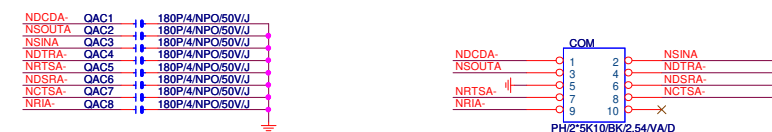
Hardware Monitor circuits

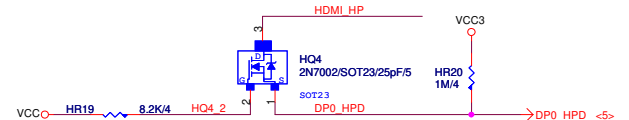
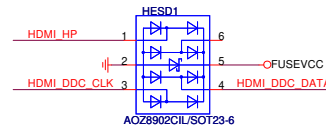
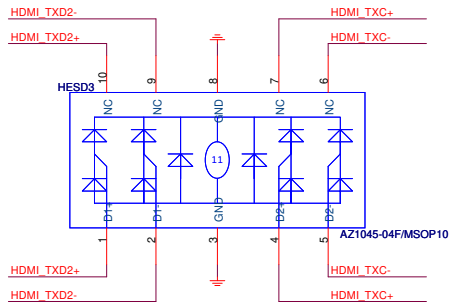
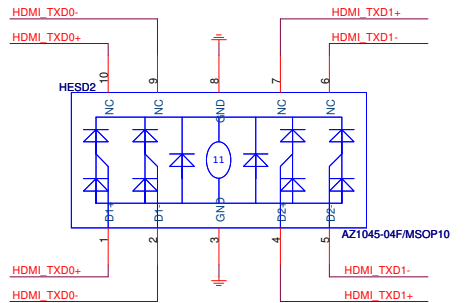
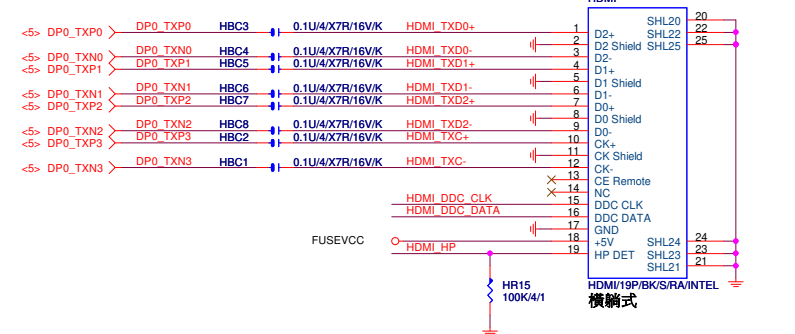
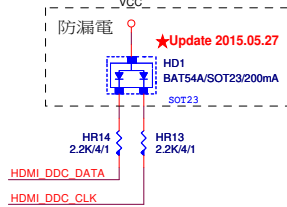
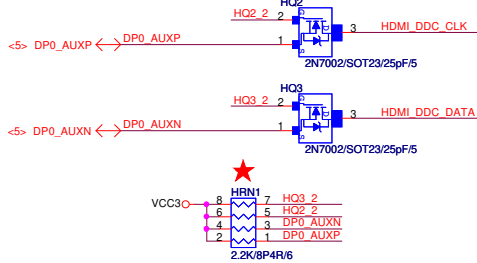
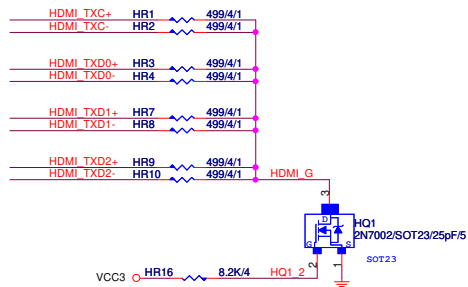


LPT PORT



R&D技術通報151 有使用PRINT PORT的
MODEL，需使用新料號：10HP2-118728-72R。(CHIP IT8728F/EX (GB) ITE/SMD
QFP128 PRINTPORT SORTING)料件。串電阻33 ohm改為68 ohm。

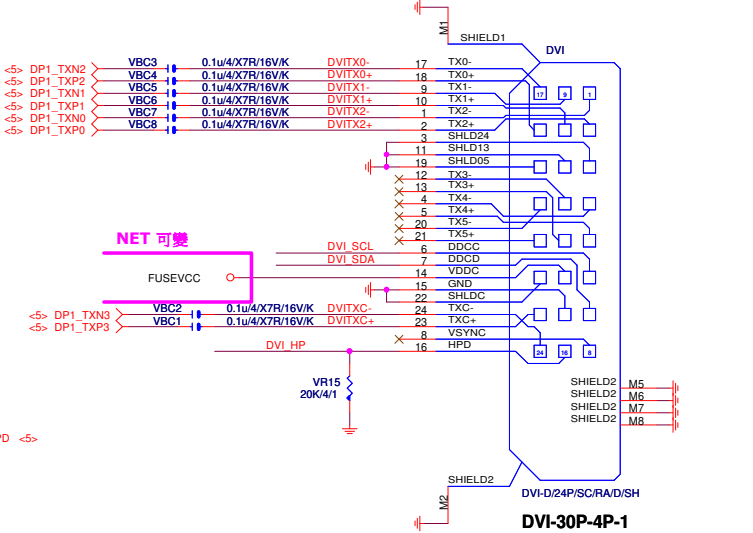
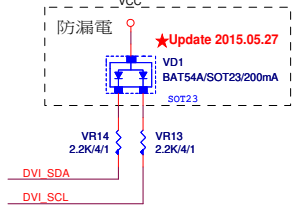
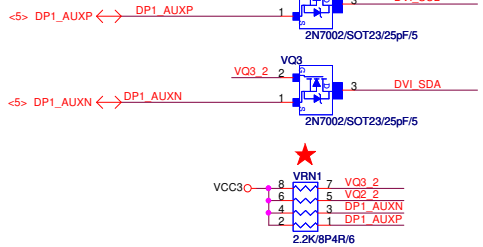
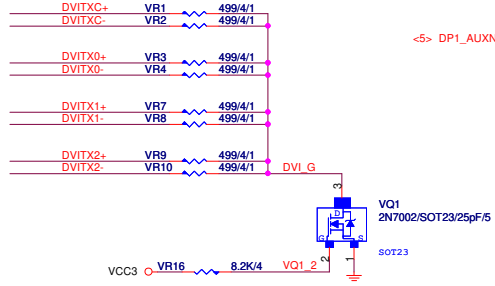




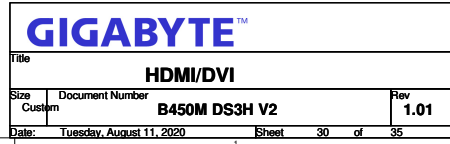
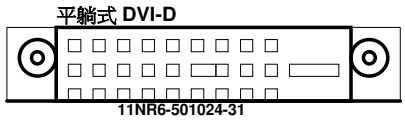
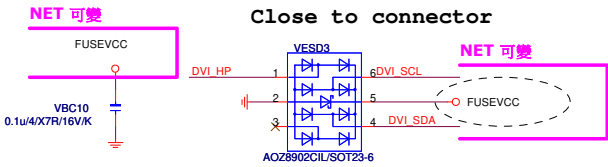
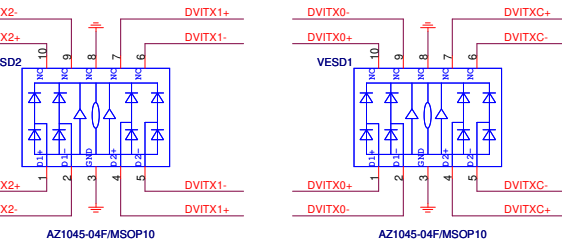
Rev: 0.73

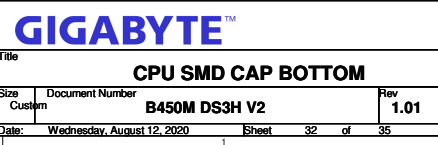
DVI CONN

DVI: 20/4/6/4/20
Impedance=85 +- 17.5%

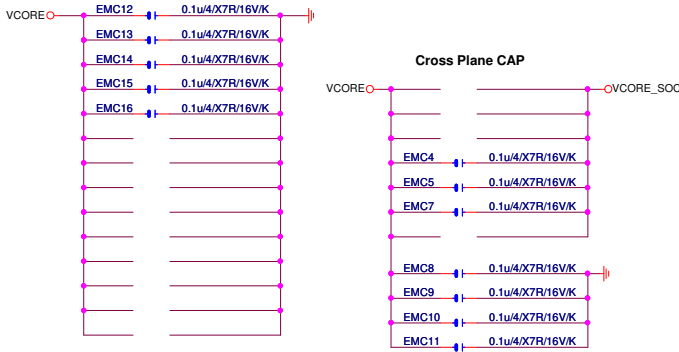
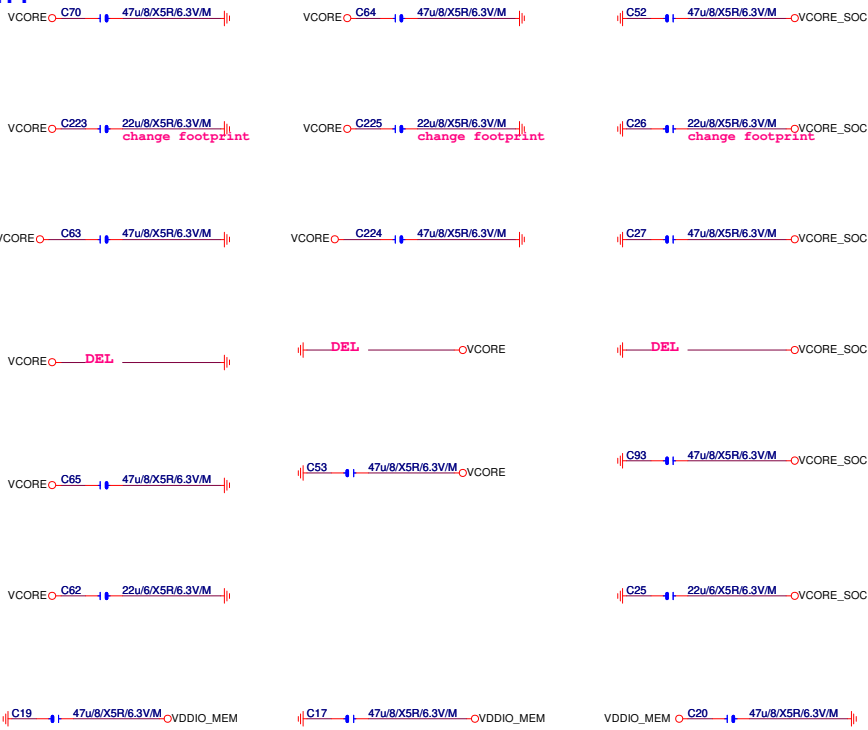


Close to connector





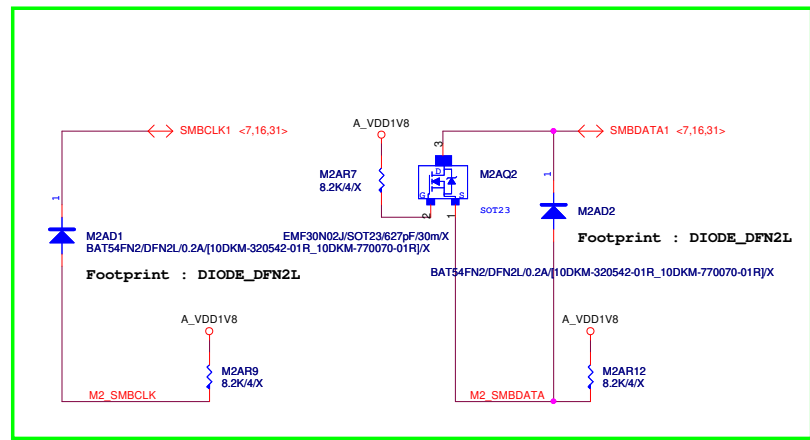
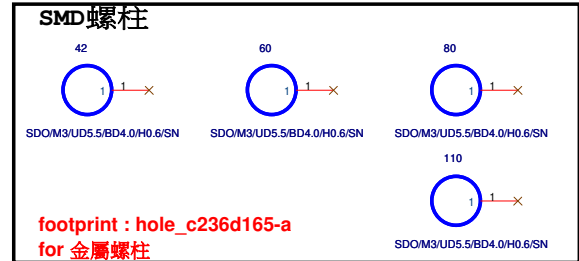
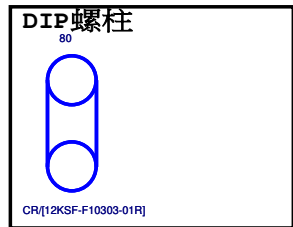
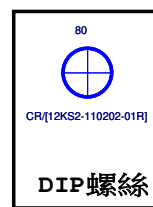
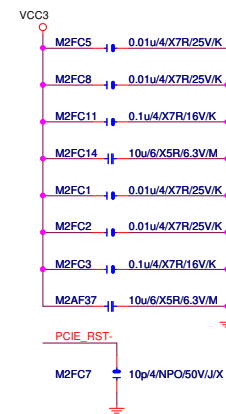
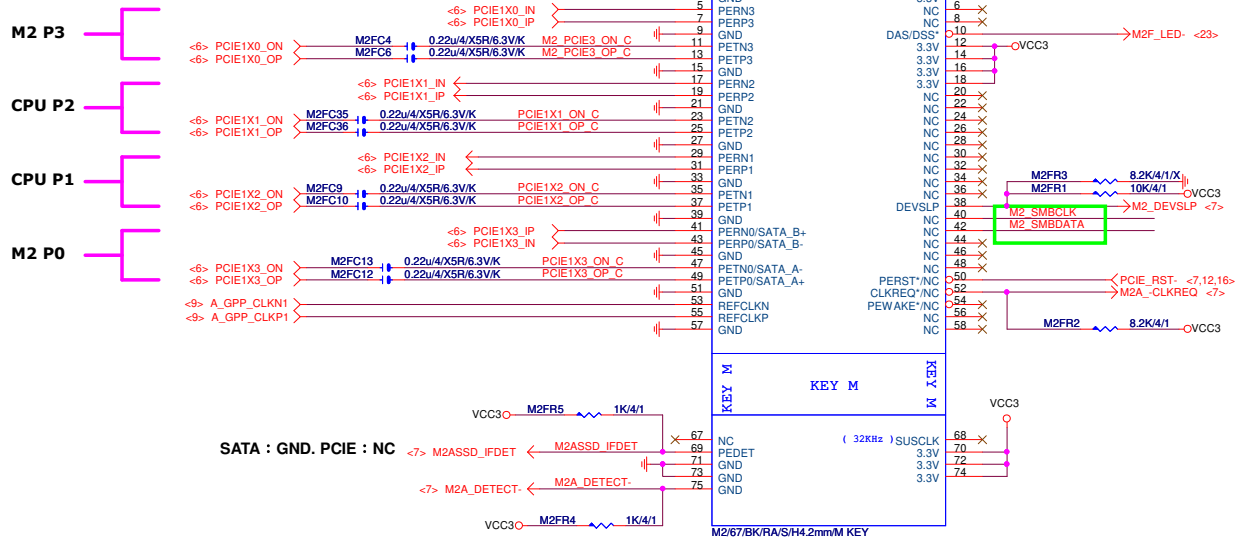
CPU TOP CAVITY

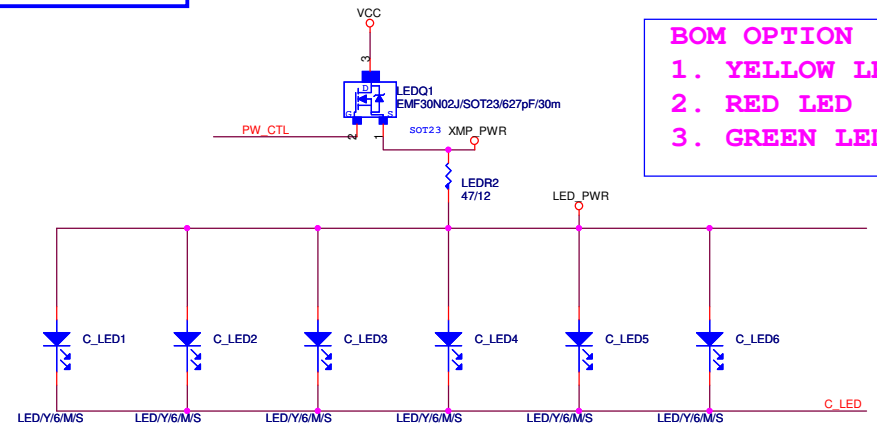


GIGABYTE™

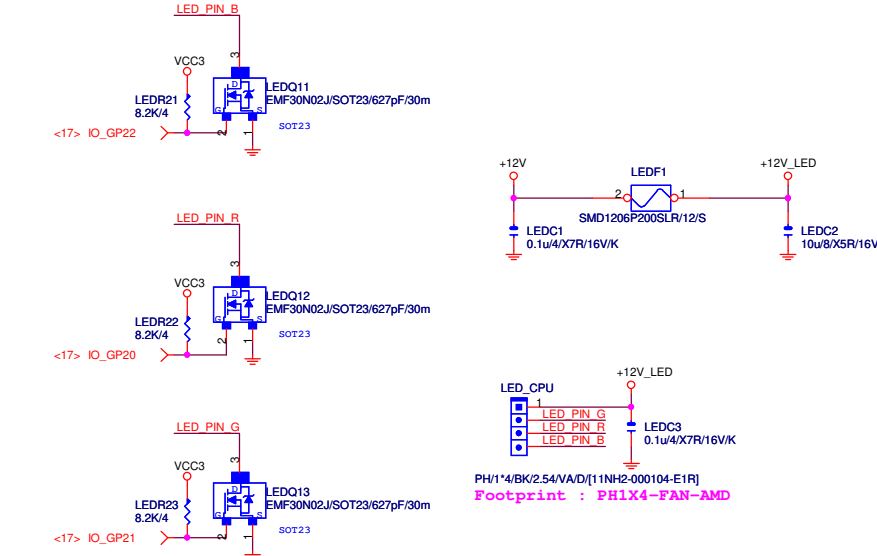
Title			
CPU SMD CAP TOP			
Size	Document Number		Rev
Custom	B450M DS3H V2		1.01
Date:	Tuesday, August 11, 2020	Sheet	33 of 35

Rev 0.5





RGB LED CONTROL

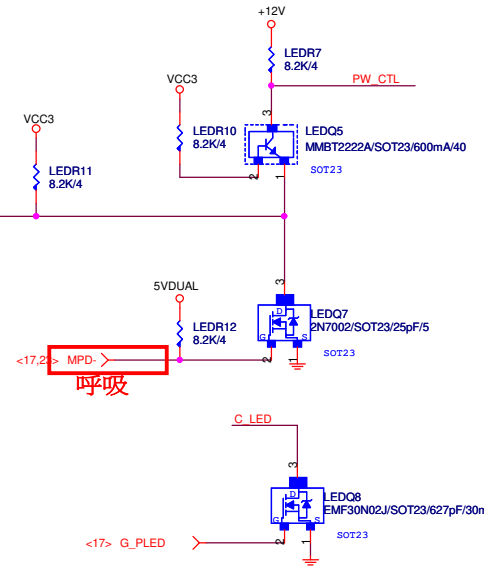


- BOM OPTION :**
- 1. YELLOW LED : LED/Y/6/M/S
 - 2. RED LED : LED/R/H/0603/S
 - 3. GREEN LED : LED/G/0603/S

Ambient LED Control

	IO_GP95	IO_GP91
Still Mode	H	L
OFF Mode	L	L
Pluse Mode	H	BREATH

17> G_PLED
ON/OFF



三色 LED Control

	IO_GP20 (R)	IO_GP21 (G)	IO_GP22 (B)
Blue	L	L	H
Green	L	H	L
Light Blue	L	H	H
Red	H	L	L
Pink	H	L	H
Light Green	H	H	L
White	H	H	H
Cycle Mode	順序:Blue-Green-Light Blue-Red-Pink-Light Green-White 切换間隔時間為 1 秒		

www.teknisi-indonesia.com

GIGABYTE™

Title: Amient Single LED

Size: Custom Document Number: B450M DS3H V2 Rev: 1.01

Date: Tuesday, August 11, 2020 Sheet: 35 of 35